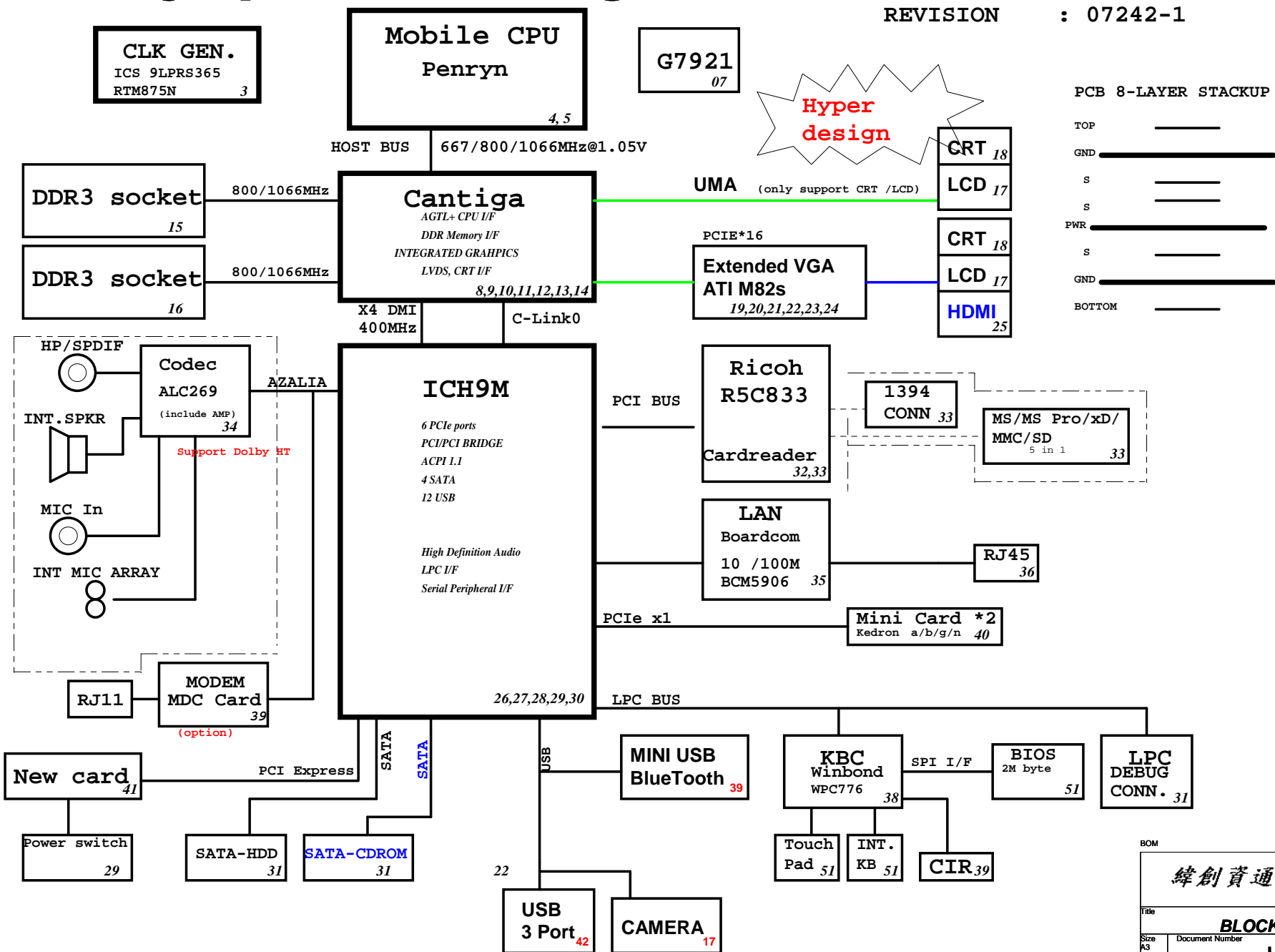


Olympus Block Diagram

Project code: 91.4Y701.001

PCB P/N :

REVISION : 07242-1



SYSTEM DC/DC	
ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)
SYSTEM DC/DC	
TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)
TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5308 39	
3D3V_S0	2D5V_S0 (300mA)
CHARGER	
BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC	
ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
NB DC/DC	
ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
SC411 48	
DCBATOUT	1D5V_S3

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLOCK DIAGRAM

Size

Document Number

LT32P

Rev

Date: Wednesday, June 18, 2008

Sheet 1 of 53

Page 1 of 33

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Configl bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE configl bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the 'No Reboot' mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:The Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSPLVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

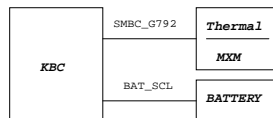
Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present: PCIE disabled

NOTE:

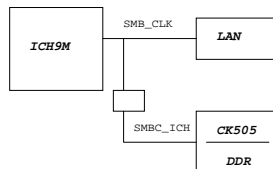
- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1



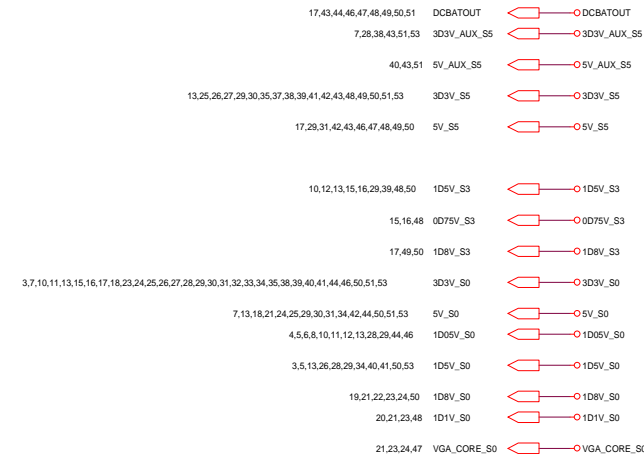
PCI Routing

page 17

IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0 0

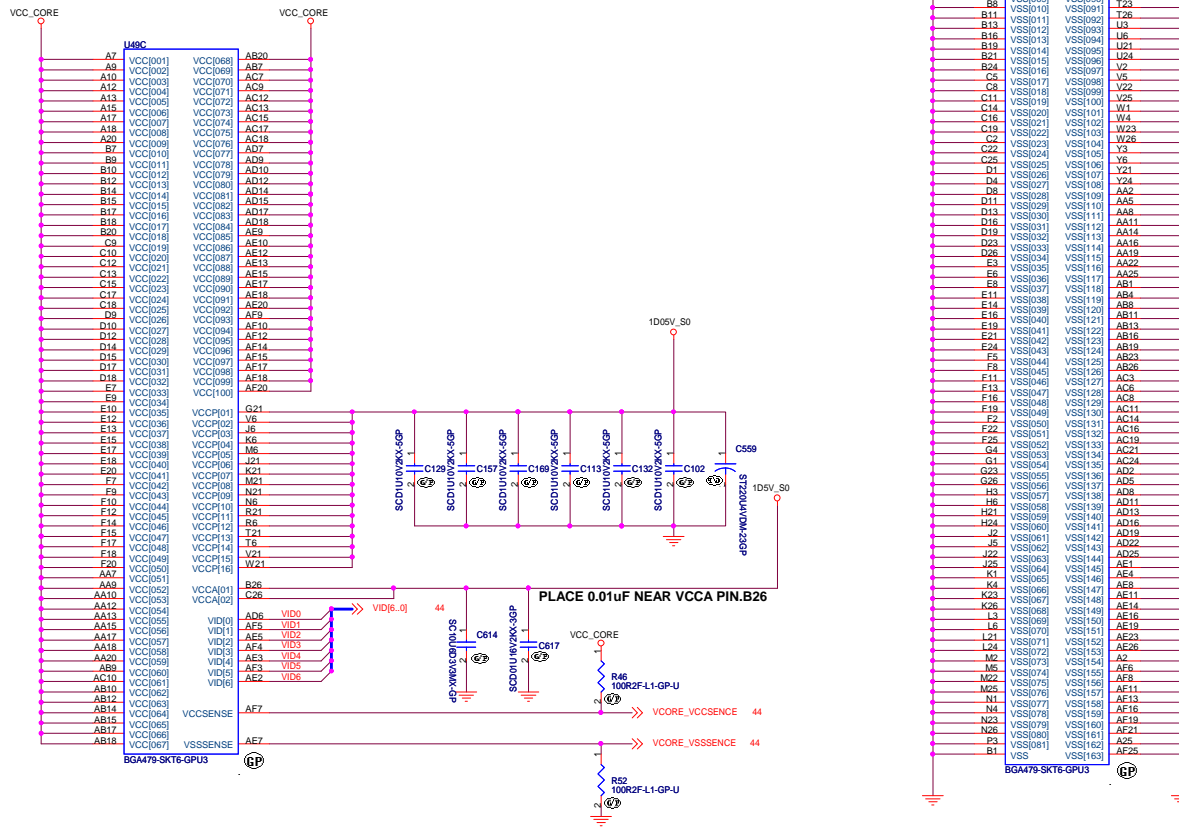
PCIE Routing

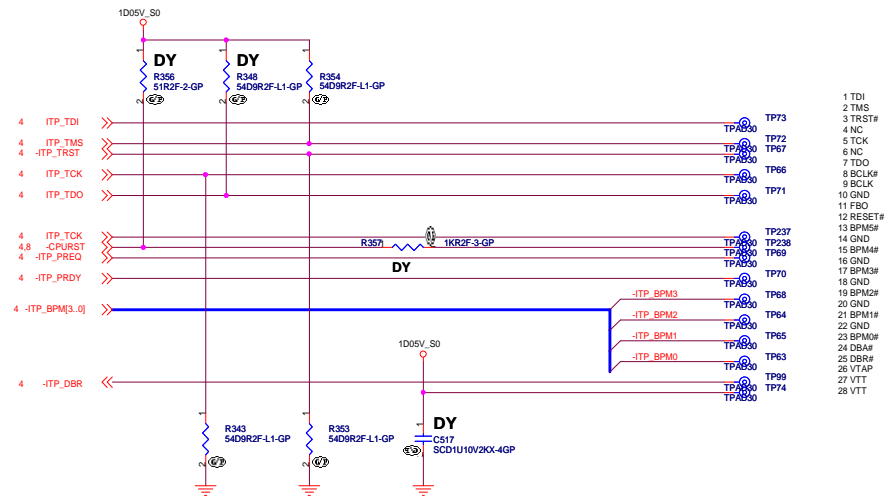
LANE2	MiniCard WLAN
LANE3	NewCard WLAN



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Title Reference	
Size C	Document Number
Olympus Date: Wednesday, July 09, 2008 Sheet 2 of 53	
Rev	-1





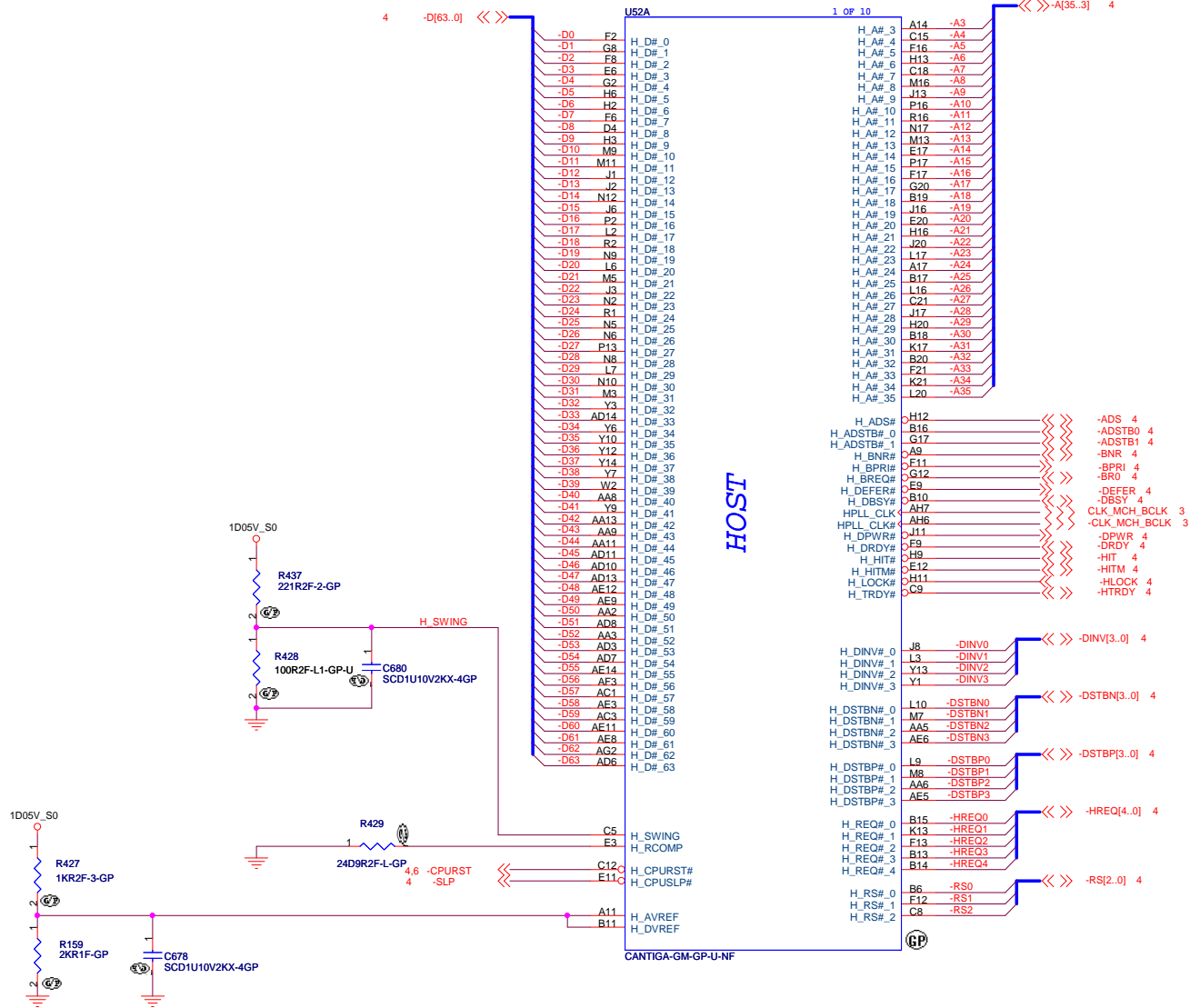
(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

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ITP CONN			
Size C	Document Number	Olympus	Rev -1
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Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

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Title	
Cantiga(1/7):HOST I/F	
Size	Document Number
A3	Olympus
Date: Wednesday, June 18, 2008	Sheet 8 of 53

15 M_A_DQ[63:0] << >>

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M_A_DQ2 AN38 SA_DQ_2
M_A_DQ3 AM38 SA_DQ_3
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M_A_DQ5 AJ40 SA_DQ_5
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CANTIGA-GM-GP-U-NF

DDR SYSTEM MEMORY A

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SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_MA_0
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BG18 M_A_BS1 15
AT25 M_A_BS2 15
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BD20 M_A_CAS 15
AY20 M_A_WE 15

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AY41 M_A_DM2
AU39 M_A_DM3
BB12 M_A_DM4
AY6 M_A_DM5
AT7 M_A_DM6
AJ5 M_A_DM7

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BC24 M_A_A6
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CANTIGA-GM-GP-U-NF

DDR SYSTEM MEMORY B

5 OF 10
SB_BS_0
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SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

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SB_DM_2
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SB_DM_7

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BB33 M_B_BS2
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BG18 M_B_CAS
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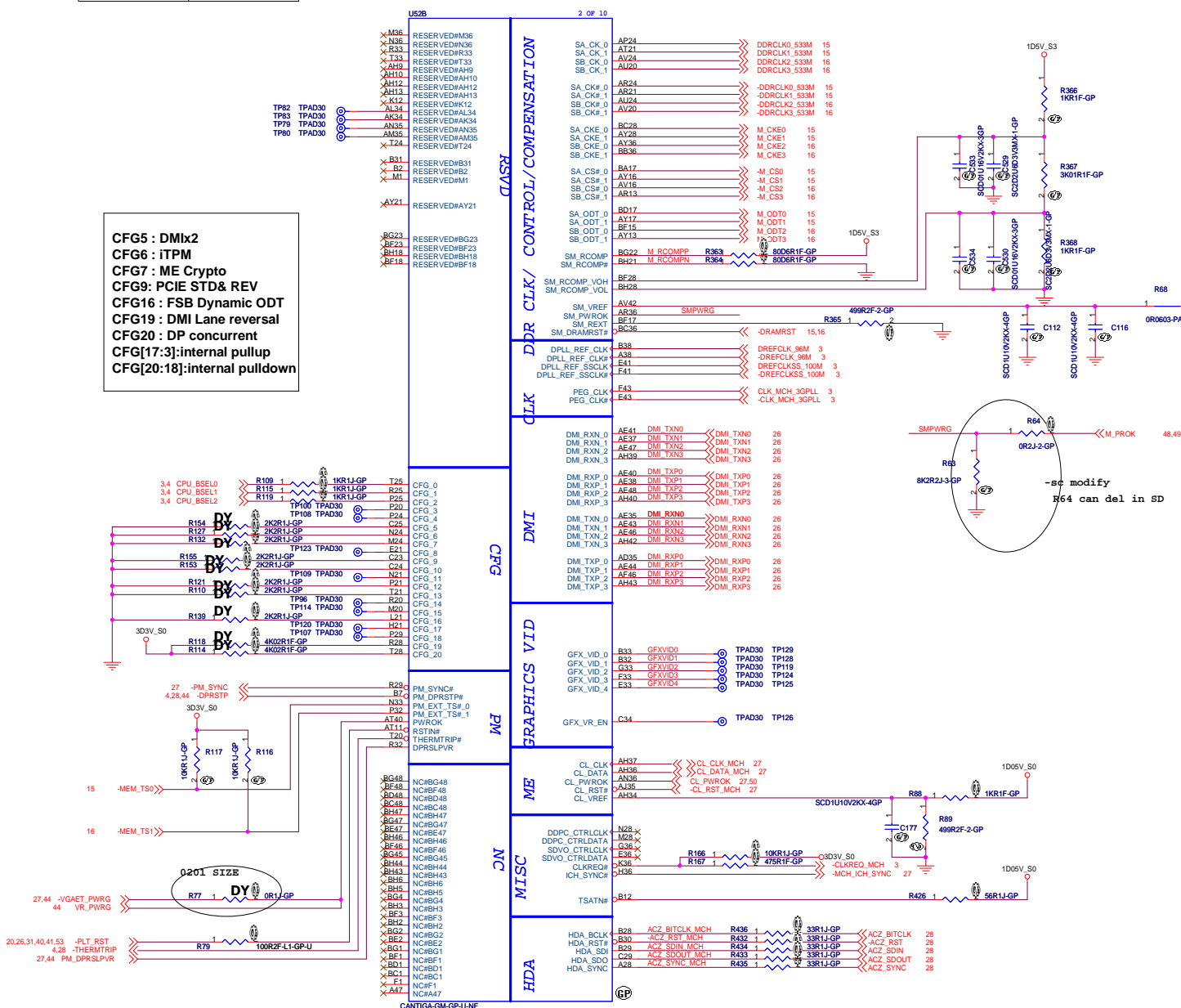
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AY33 M_B_A12
BH15 M_B_A13
AU33 M_B_A14

CP

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DImX2
 CFG6 : ITPM
 CFG7 : ME Crypto
 CFG9: PCIE STD& REV
 CFG16 : FSB Dynamic ODT
 CFG19 : DMI Lane reversal
 CFG20 : DP concurrent
 CFG[17:3]:internal pullup
 CFG[20:18]:internal pulldown



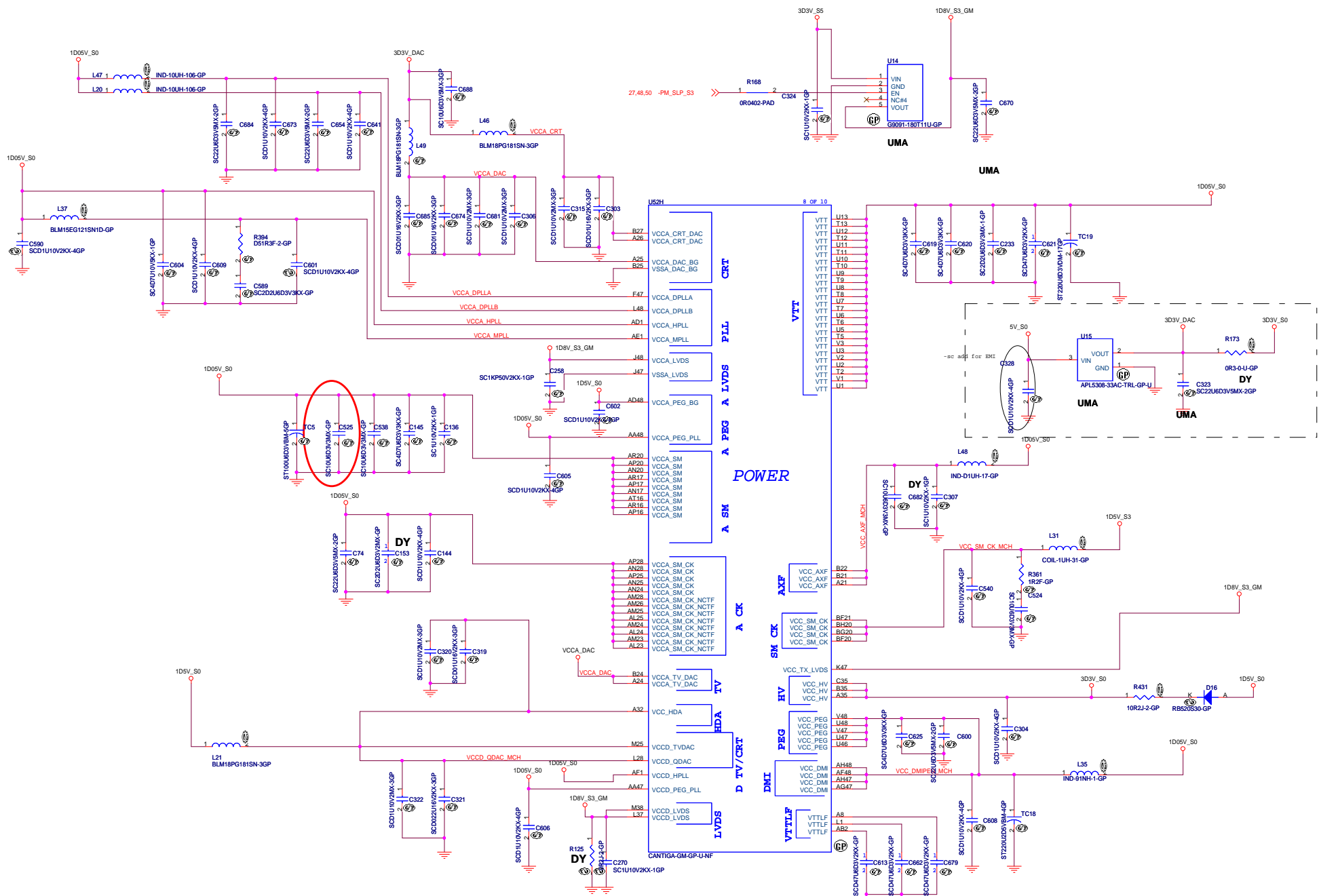
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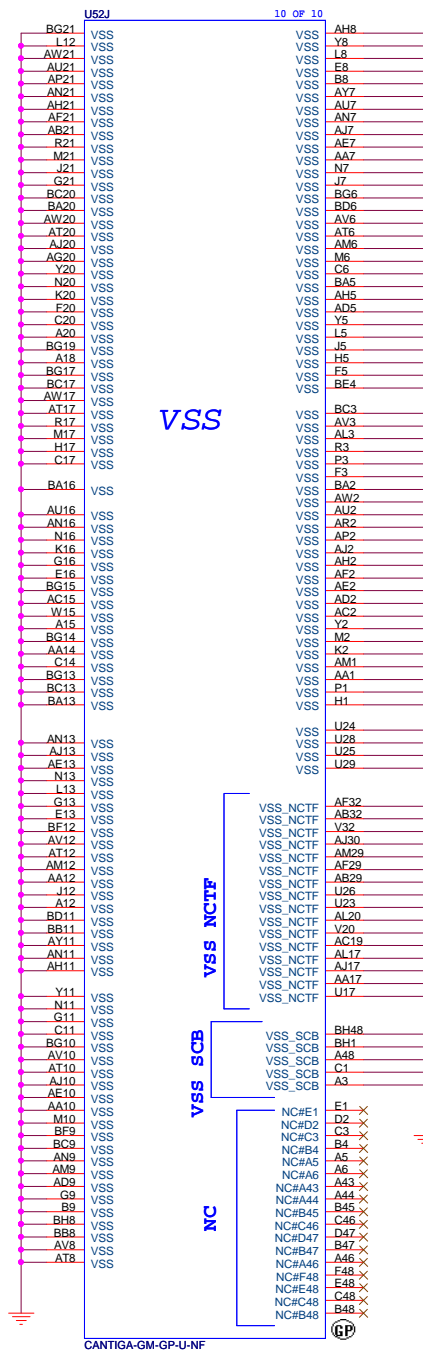
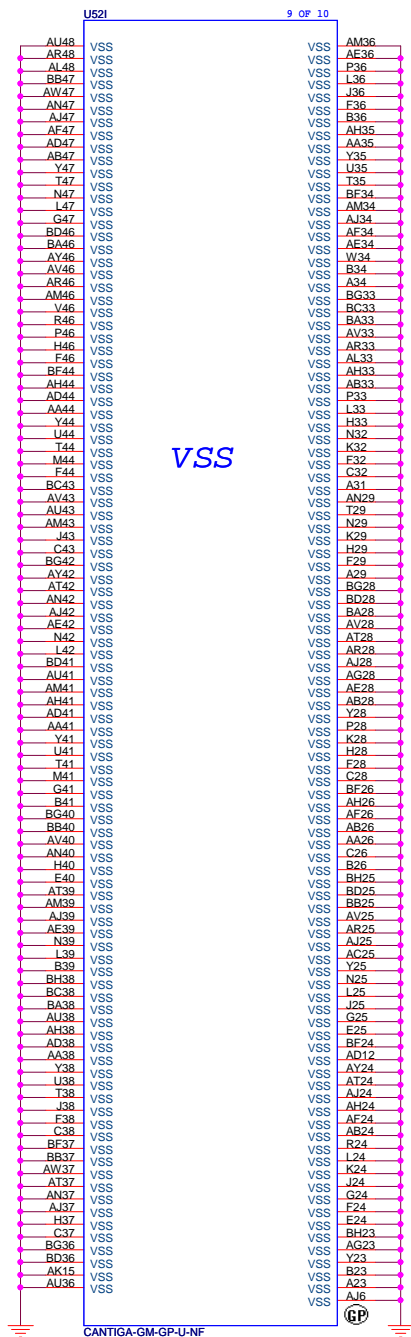
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Rev C Document Number Cantiga(3/7):DMI/PM/CFG/GF

Olympus

Date: Friday, July 04, 2008 Sheet 10 of 53





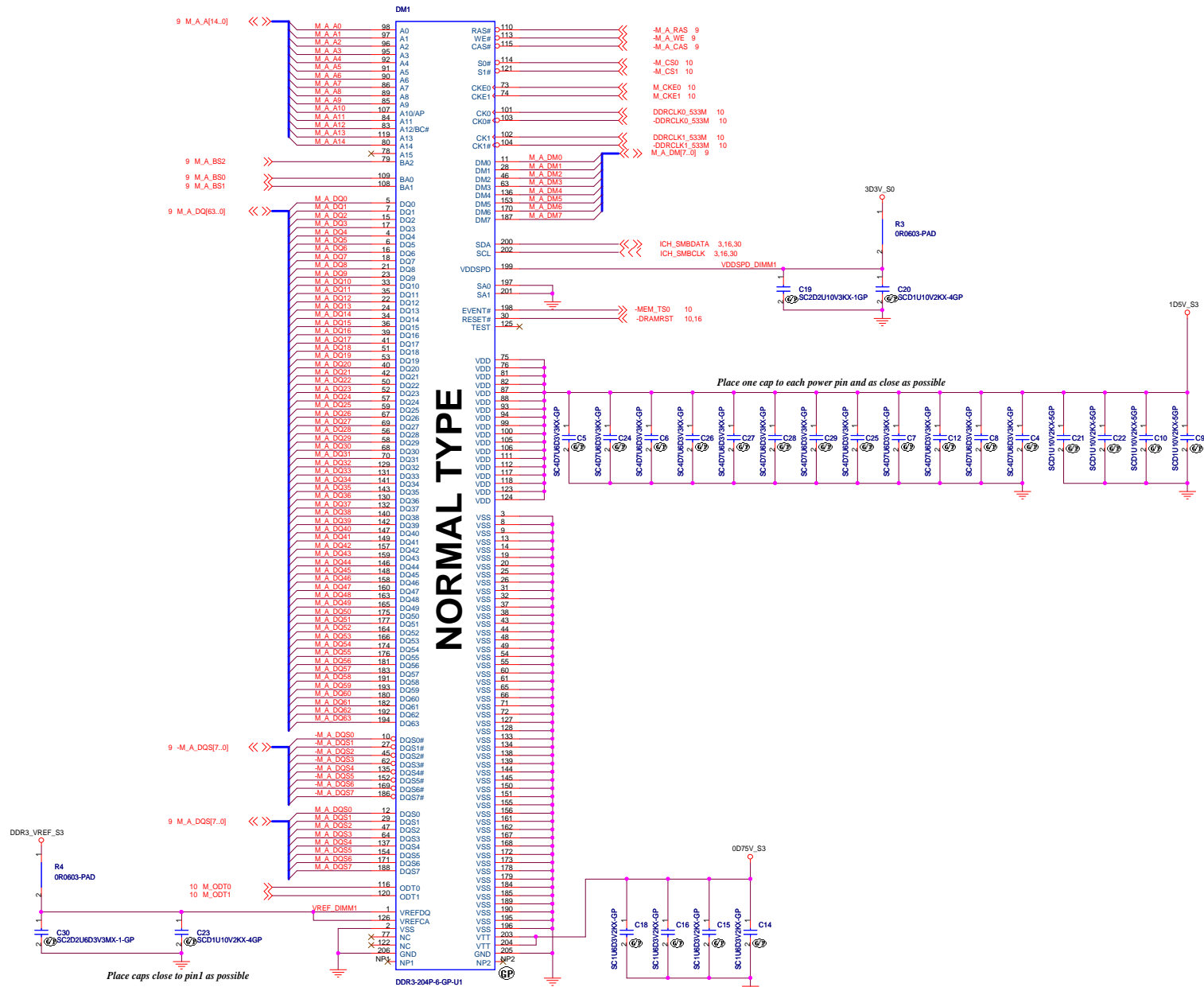
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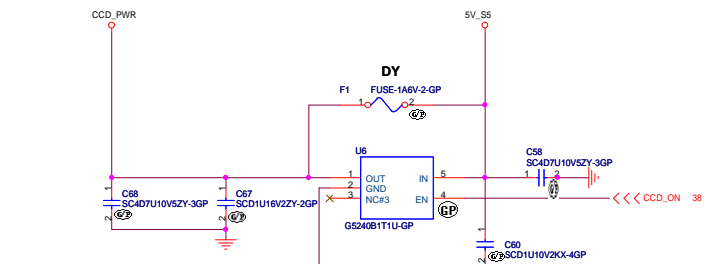
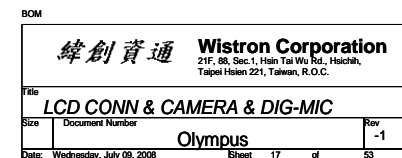
緯創資通 Wistron Corporation
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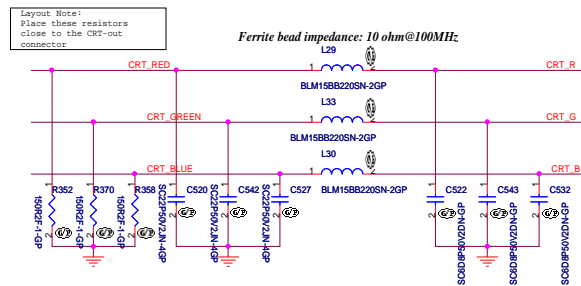
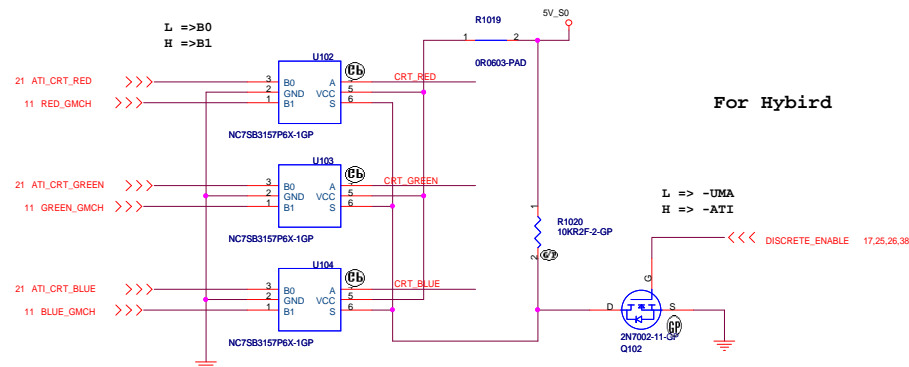
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Size: A3 Document Number: **Olympus** Rev: -1

Date: Wednesday, June 18, 2008 Sheet 14 of 53

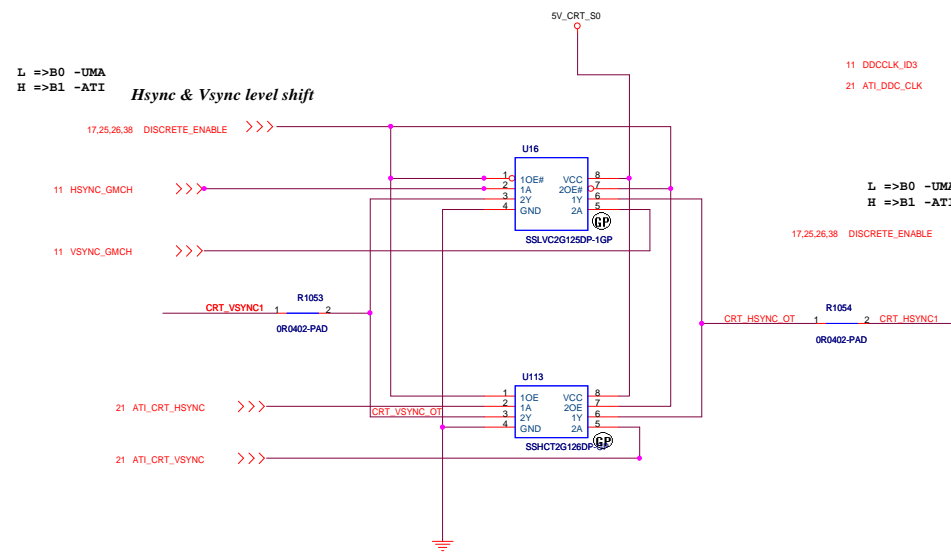


[illegible][illegible]

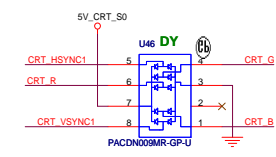
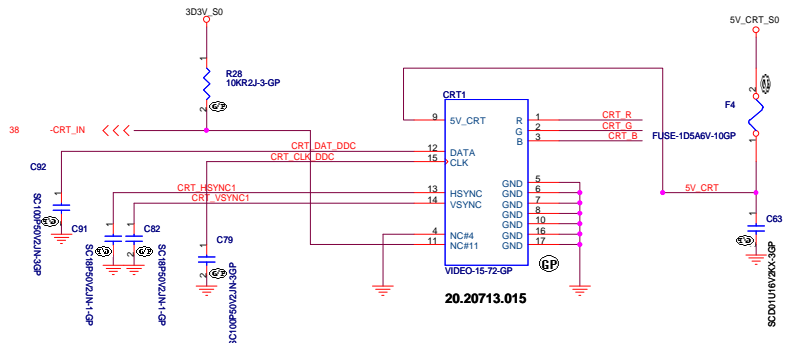


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

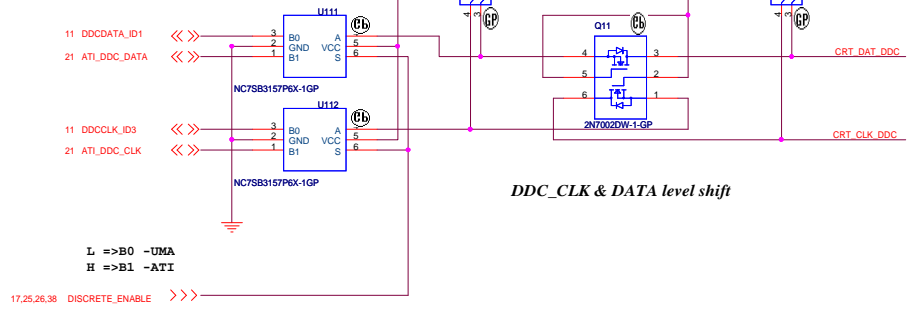
Hsync & Vsync level shift



CRT I/F & CONNECTOR



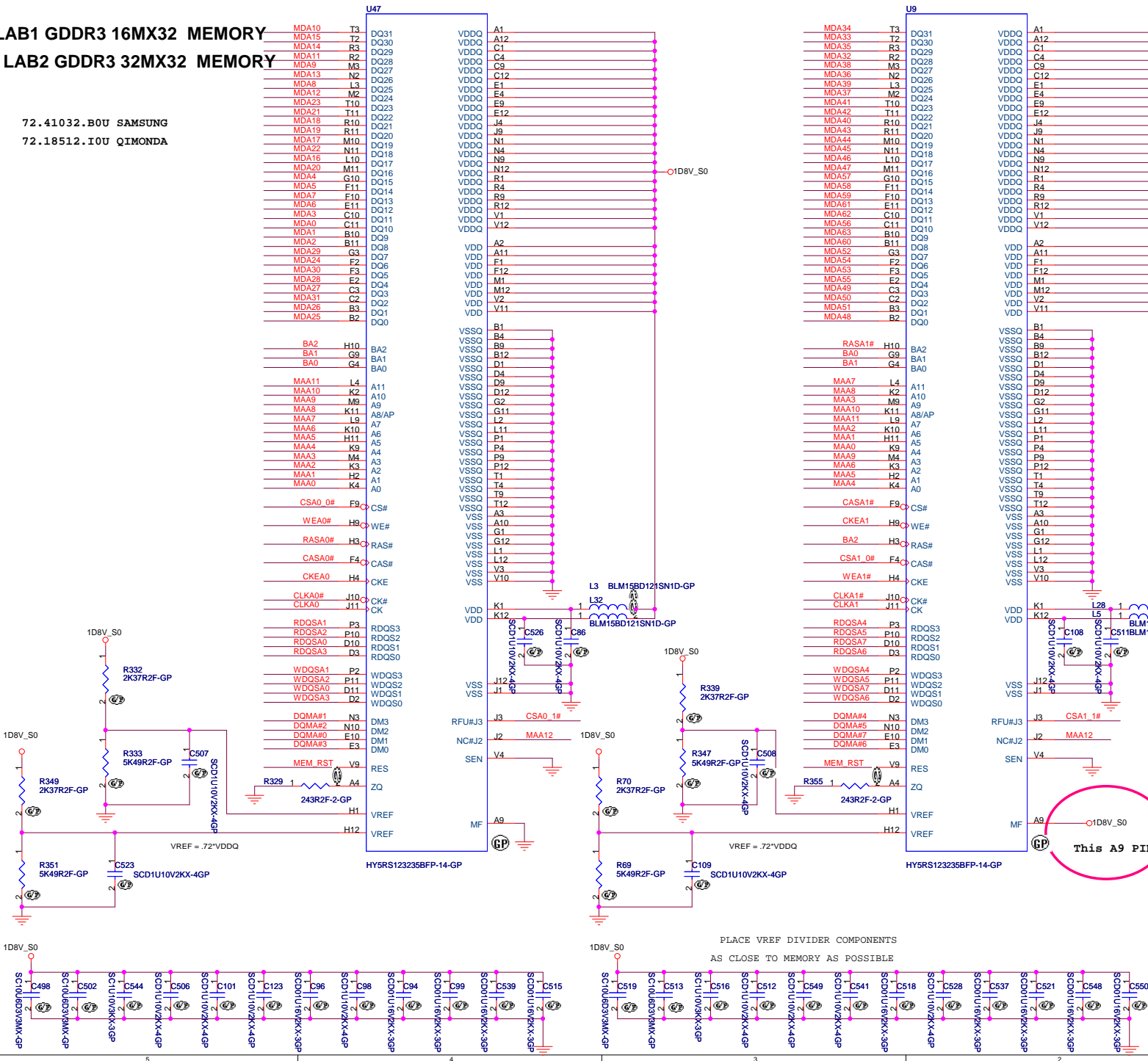
L ==> B0 -UMA
H ==> B1 -ATI



DDC_CLK & DATA level shift

LAB1 GDDR3 16MX32 MEMORY
LAB2 GDDR3 32MX32 MEMORY

72.41032.B0U SAMSUNG
72.18512.I0U QIMONDA



DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M625, M645, M715 AND M725.
SEE DATA BOOK FOR LATEST INFORMATION

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ATI M82-S VRAM(1,2)

Size A3

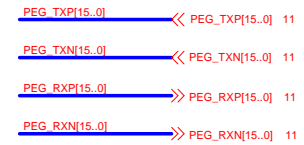
Document Number



Olympus

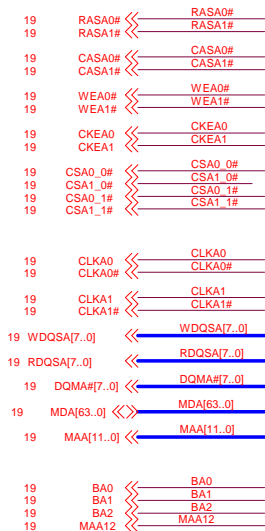
Rev -1

Date: Wednesday, July 09, 2008

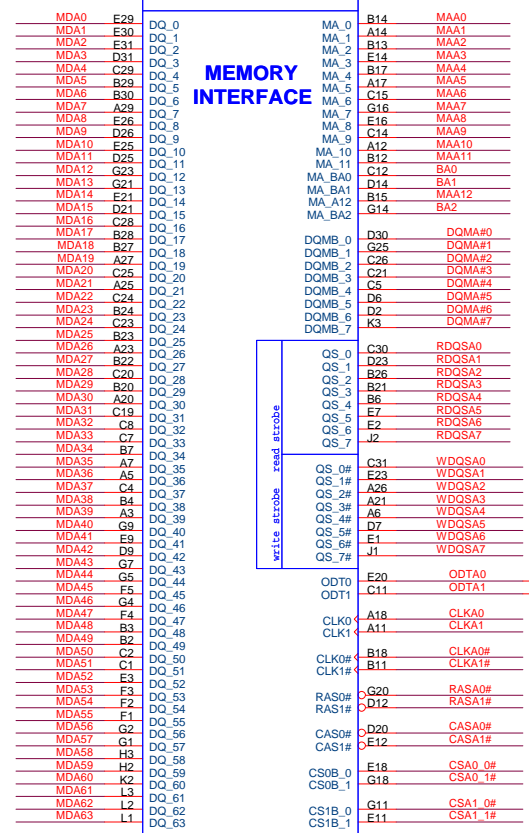
Sheet 19 of 53



 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ATI M82-S(1/6):PCIE Interface	
Size	Document Number
	
Date: Thursday, July 03, 2008	Sheet 20 of 53
Rev -1	



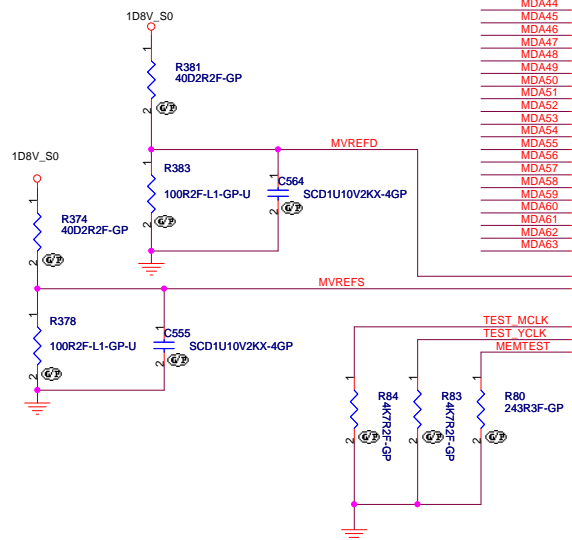
U53C 3 OF 6
Part 3 of 6
MEMORY INTERFACE



FOR DUAL RANK CONNECTIONS
USE THE CSxB_1 CHIP SELECT PINS

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



BOM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ATI M82-S(3/6):Memory Interface

Size
A3

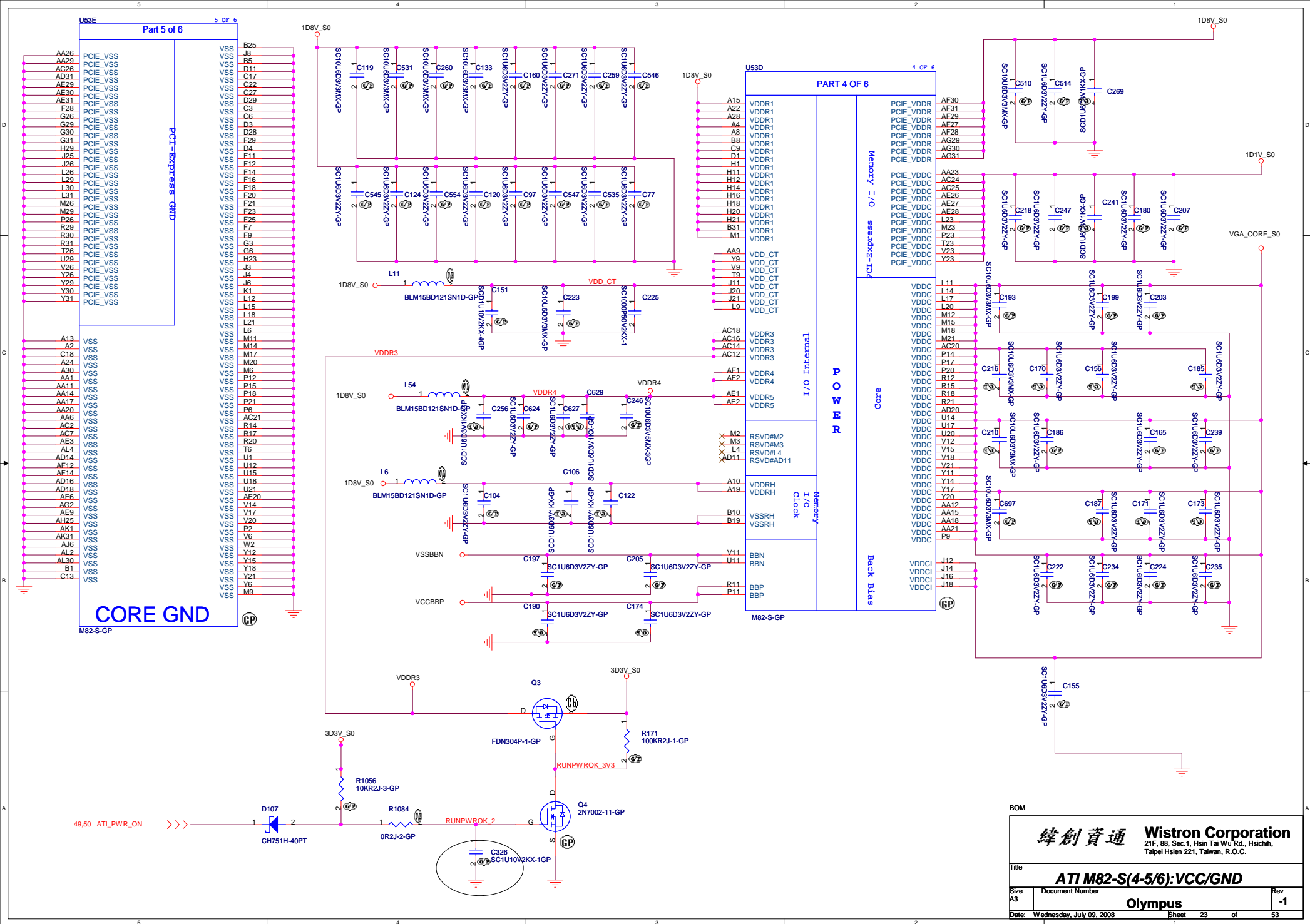
Document Number

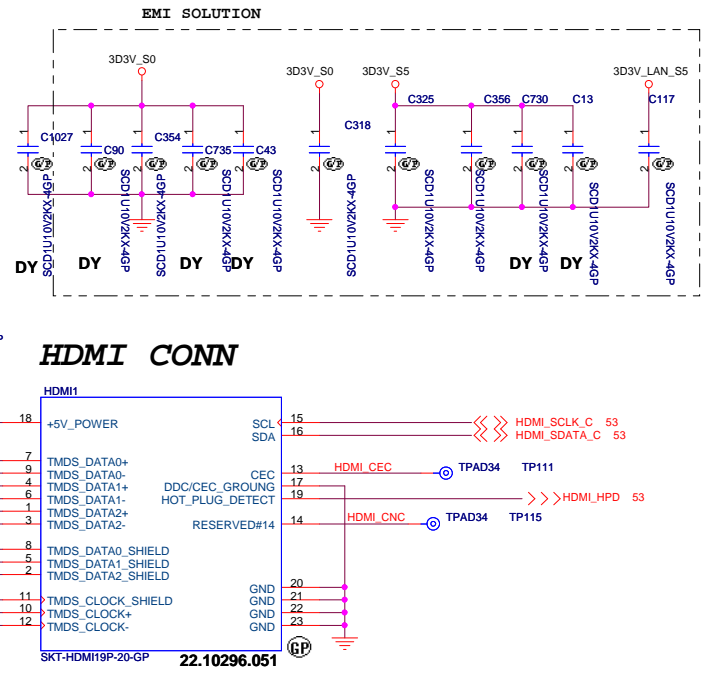
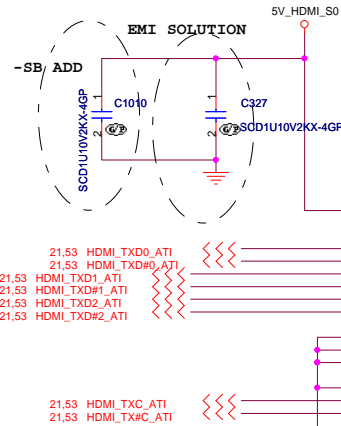
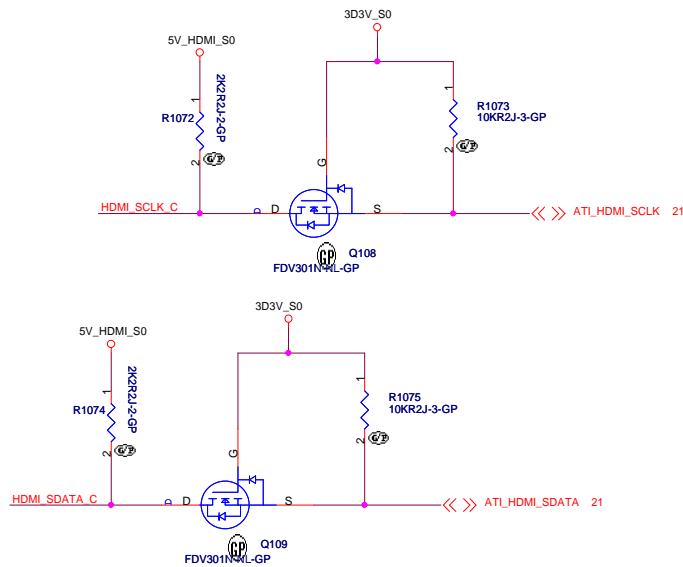
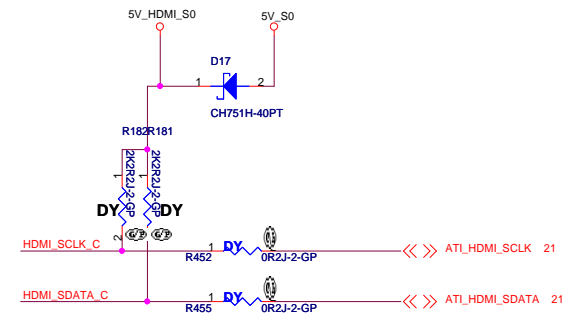
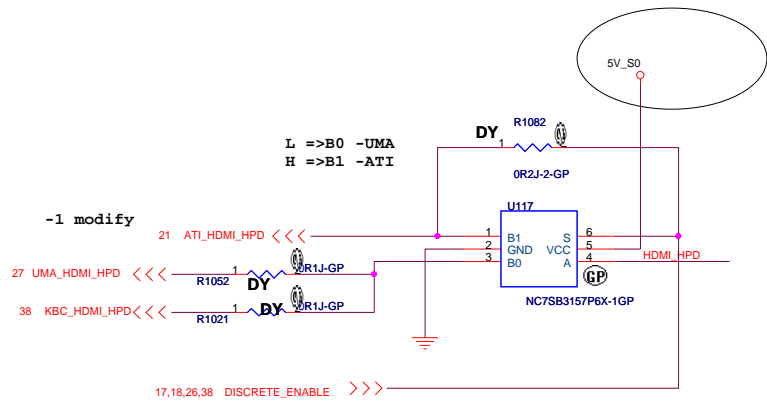
Olympus

Rev
-1

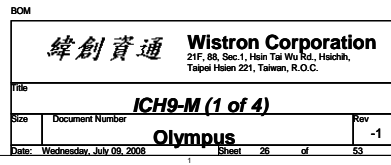
Date: Wednesday, July 09, 2008

Sheet 22 of 53

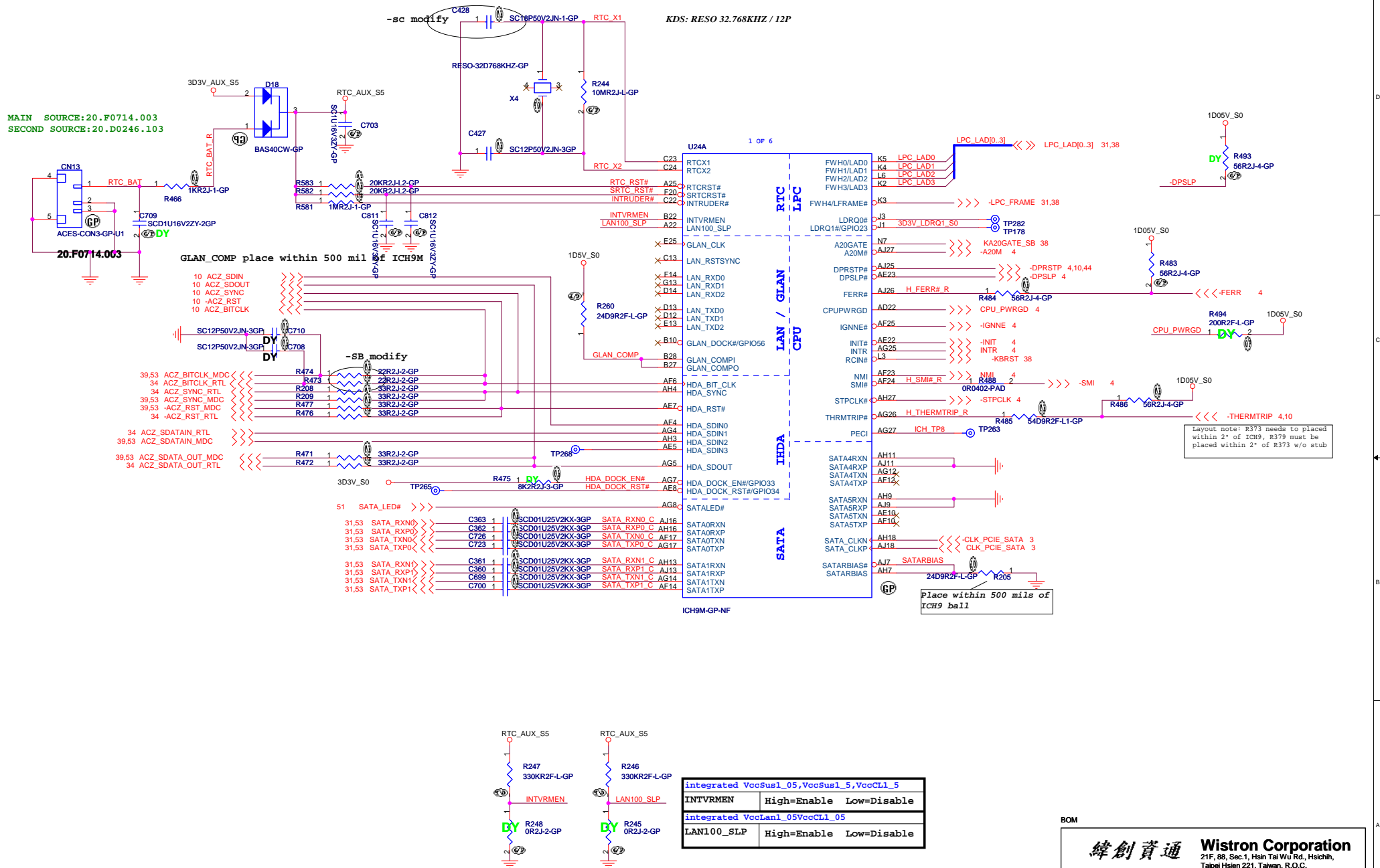


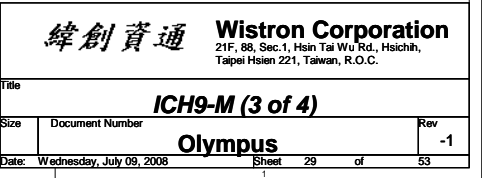


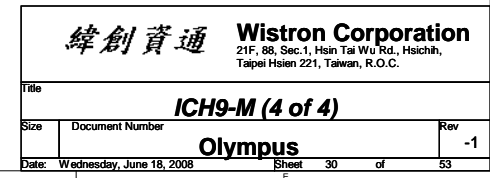
BOM		緯創資通 Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		HDMI CONN	
Size A3	Document Number	Olympus	
Date: Wednesday, July 09, 2008	Sheet 25 of 53	Rev -1	



MAIN SOURCE:20.F0714.003
SECOND SOURCE:20.D0246.103

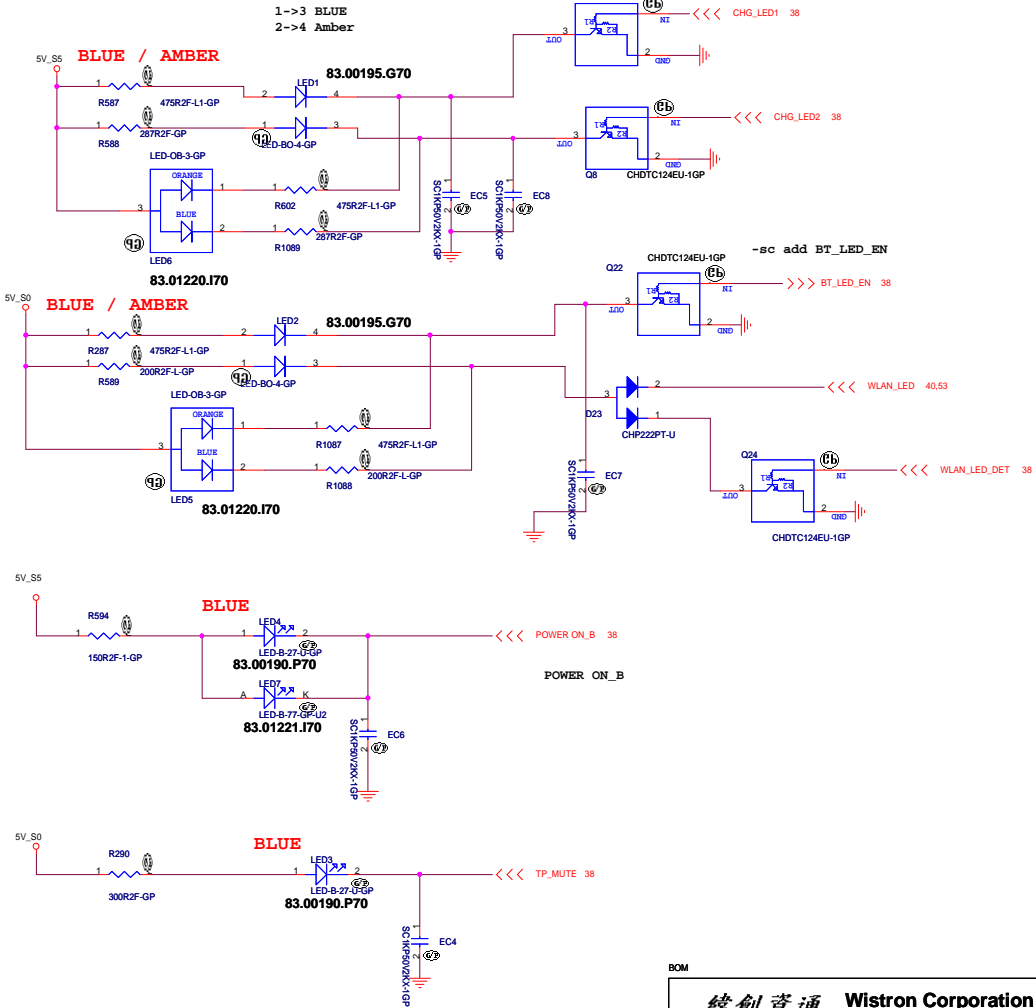
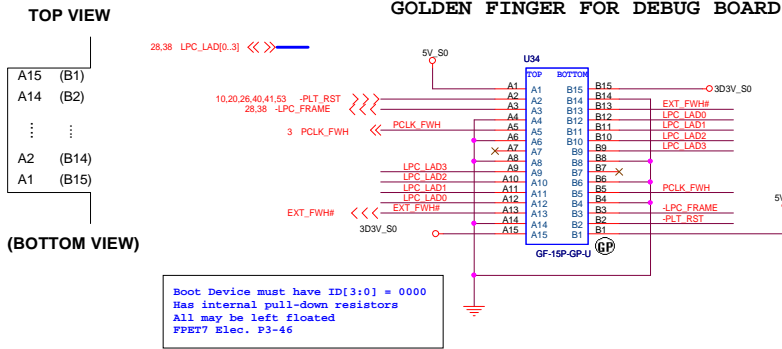
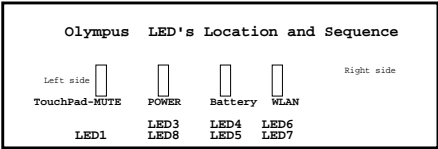
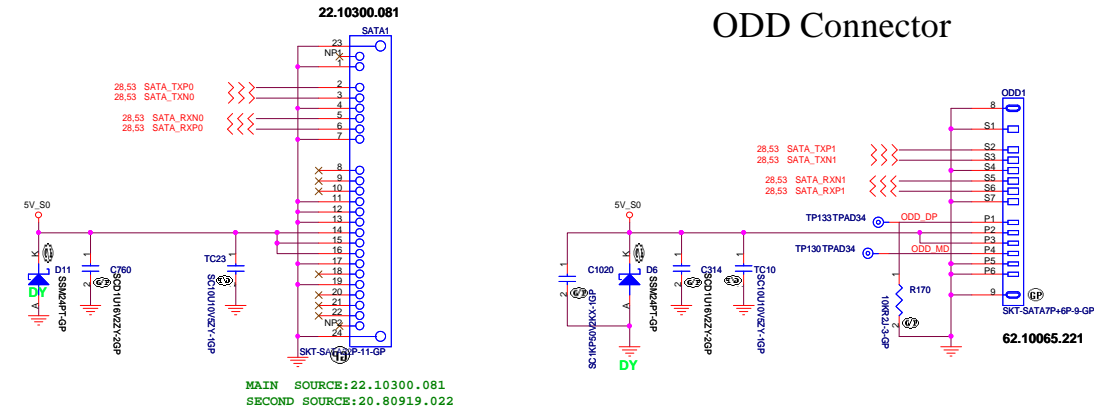


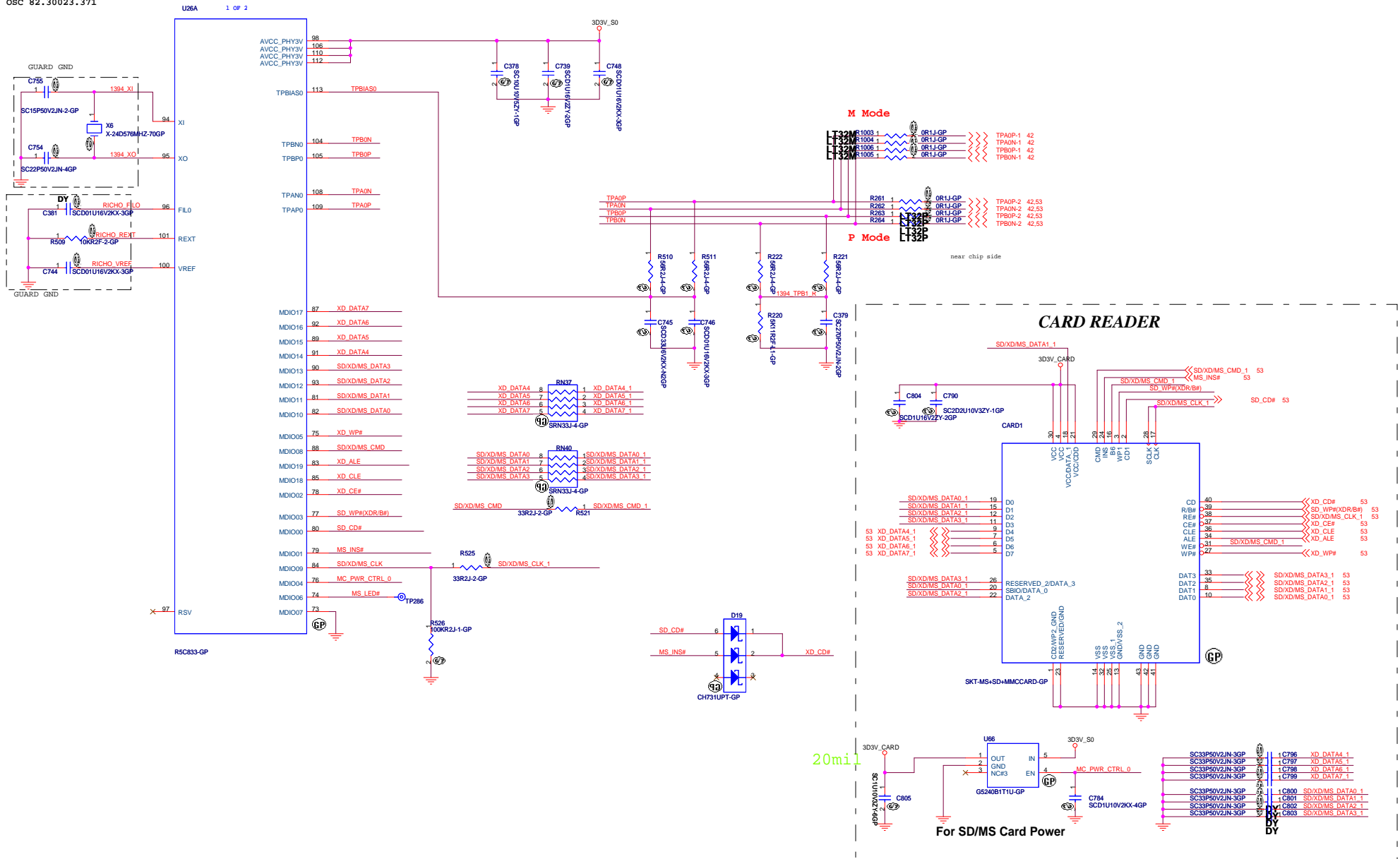


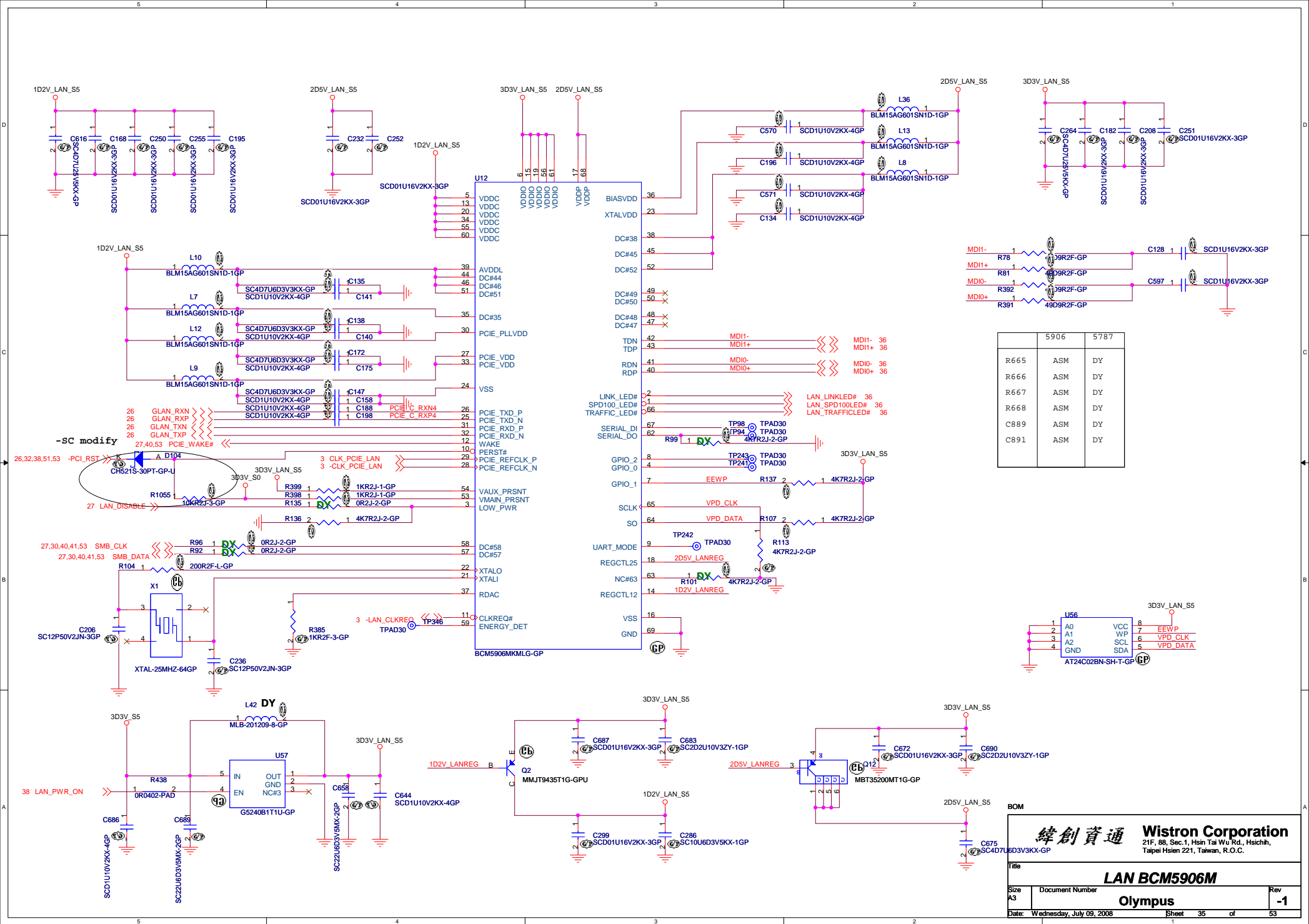


SATA HD Connector

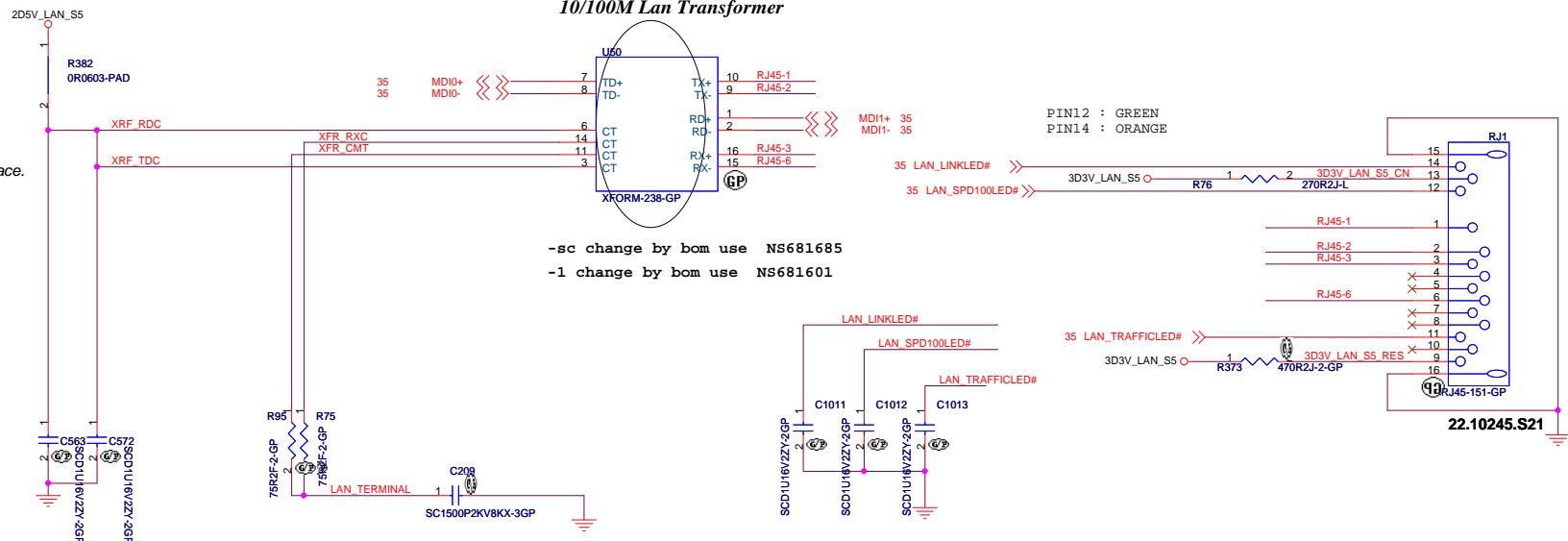
ODD Connector





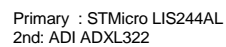


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN connector/NEW CARD/SIM			
Size A3	Document Number		Rev -1
Olympus			
Date: Wednesday, July 09, 2008		Sheet 36 of	53

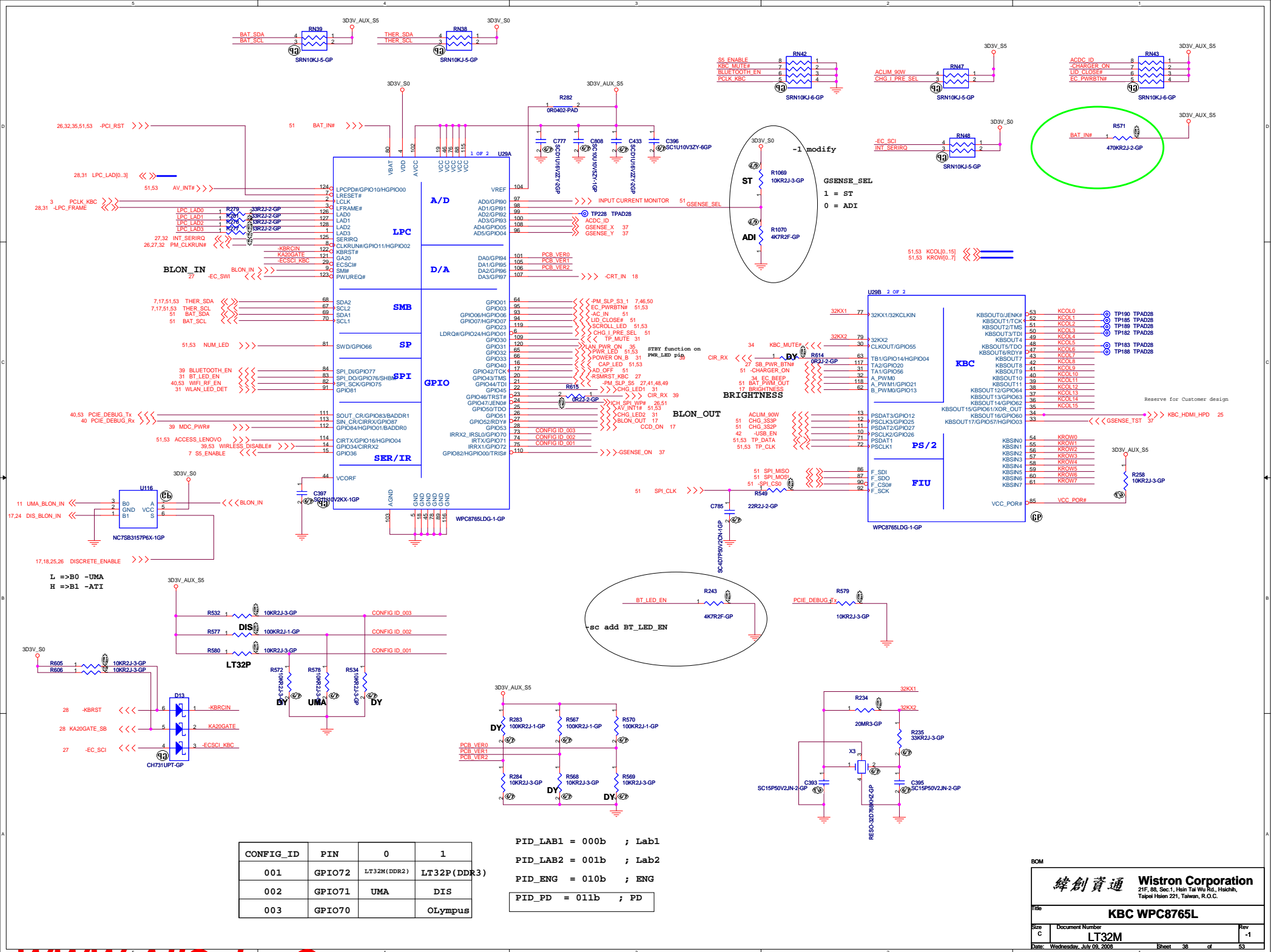


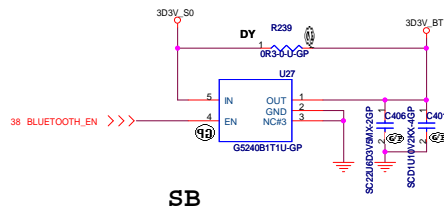
Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

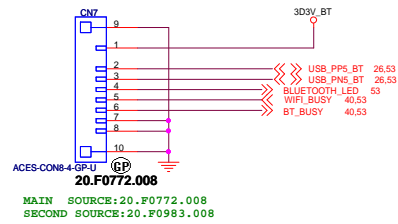
(2) Avoid routing under DCDC switching area.

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

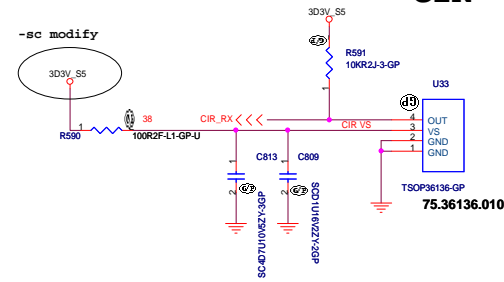




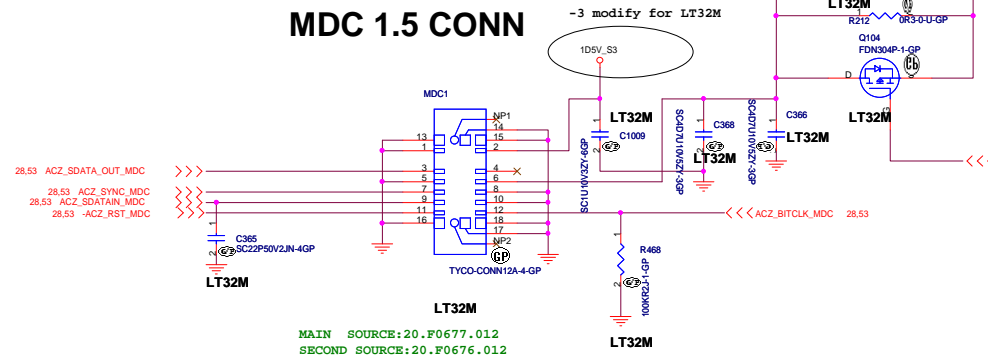
BT CONNECTOR



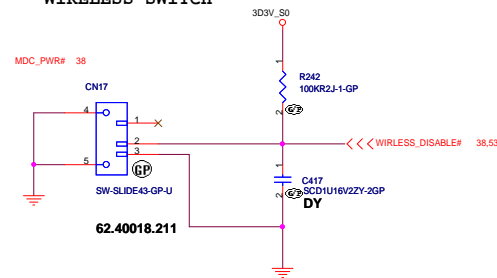
CIR



MDC 1.5 CONN



WIRELESS SWITCH



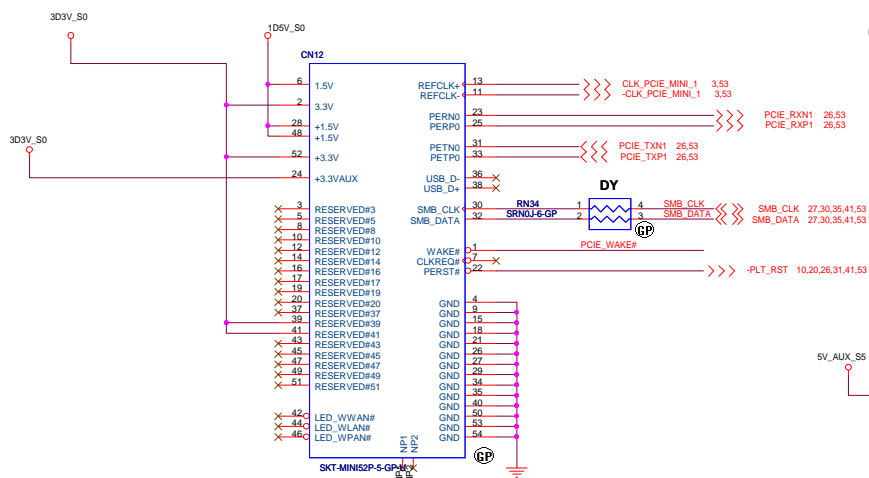
BOM

Mini PCI-E Connector

Only port-1 support USB

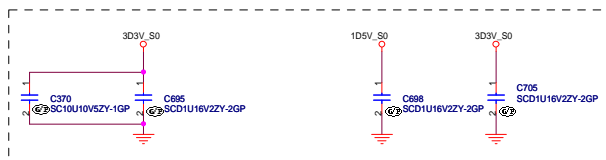
For Robson

Port-1 High



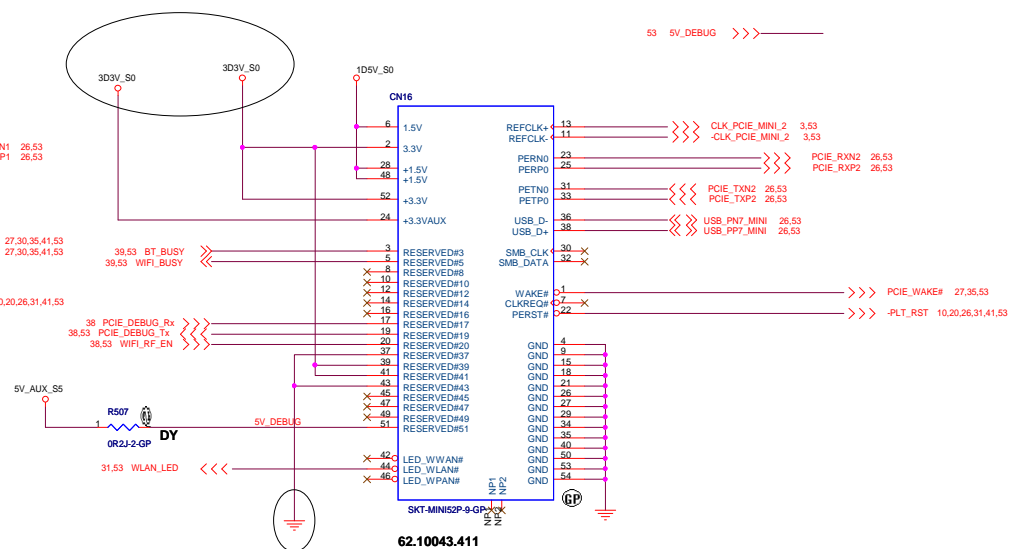
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SECOND SOURCE:20.F1107.052



Mini PCI-E Connector

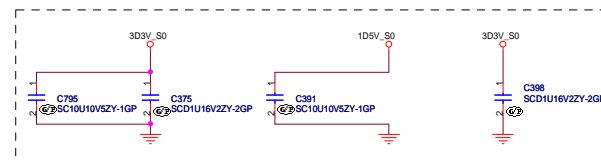
Port-2 low



62.10043.411

MAIN SOURCE:62.10043.411

SECOND SOURCE:20.F1084.052



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	
-------	--

MINI CARD CONN.

Size	Document Number	Rev
------	-----------------	-----

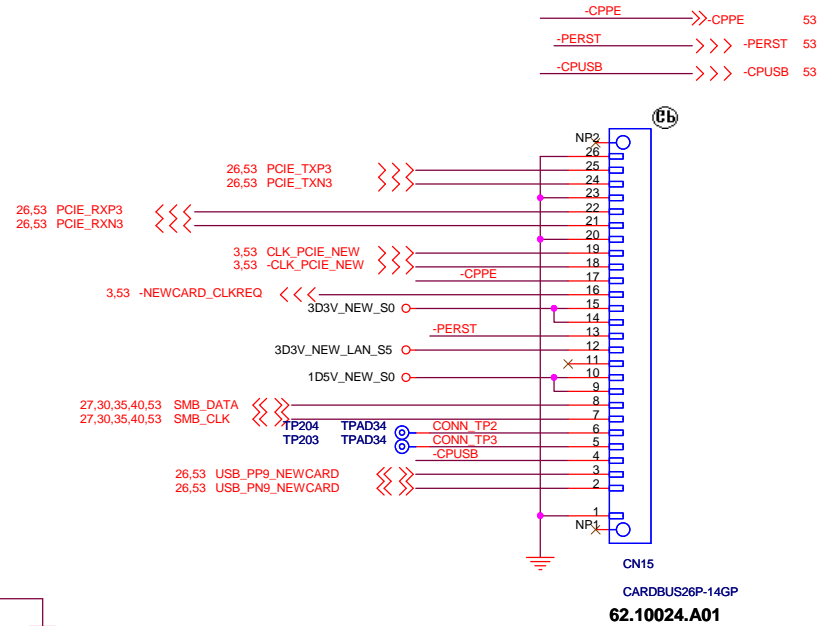
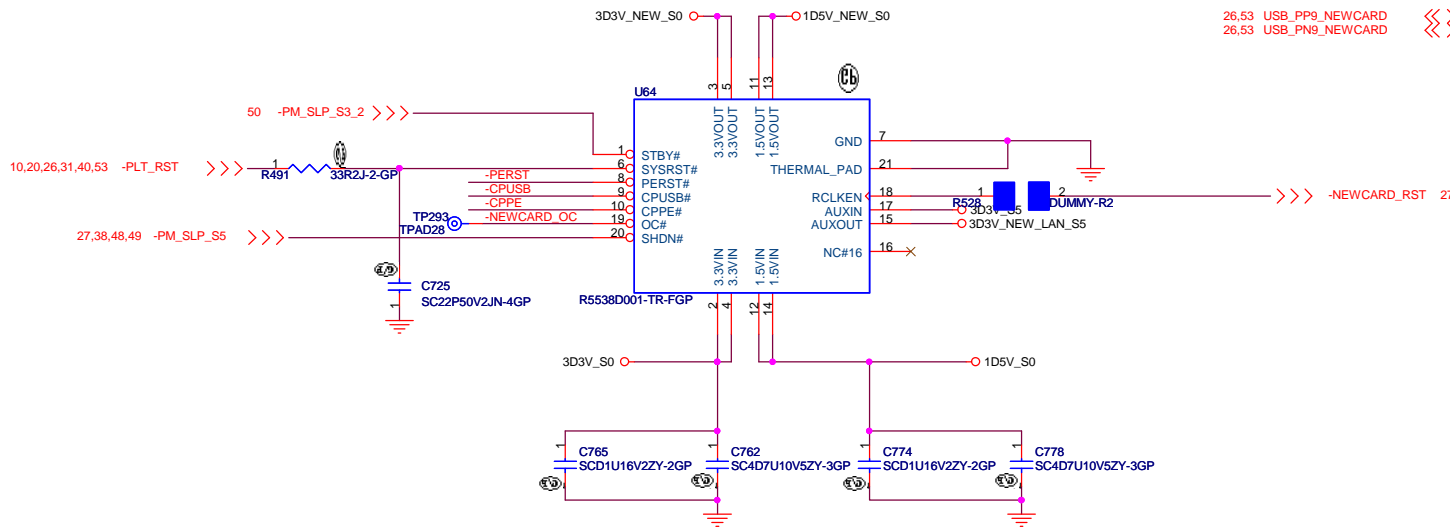
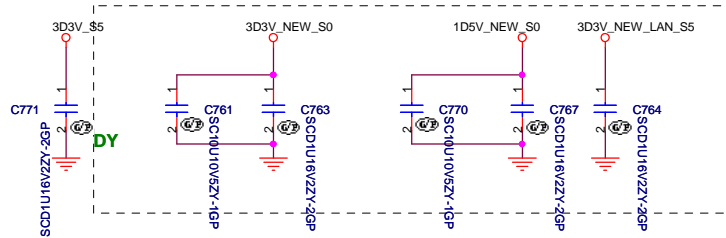
c	Olympus	-1
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Date: Wednesday, July 09, 2008 Sheet 40 of 53

NEWCARD Connector

Place them Near to Chip

Place them Near to Connector



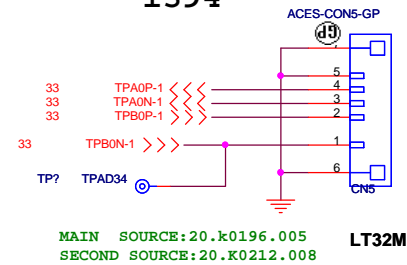
BOM

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Module NewCard			
Size	Document Number		Rev
Date: Wednesday, July 09, 2008		Sheet 41 of 53	-1

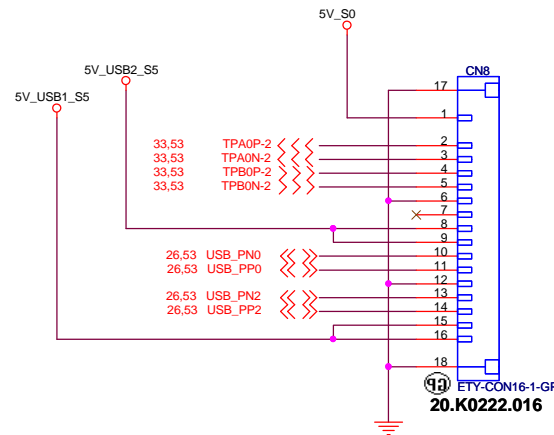
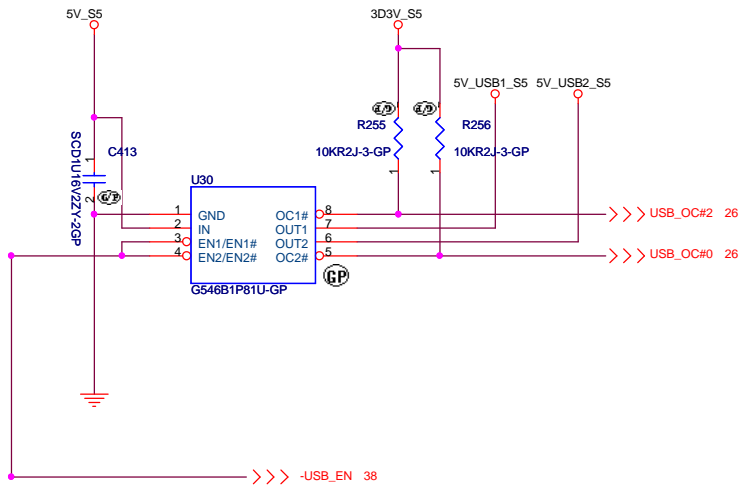
USB * 2 PORT

Low -End USB BOARD

1394

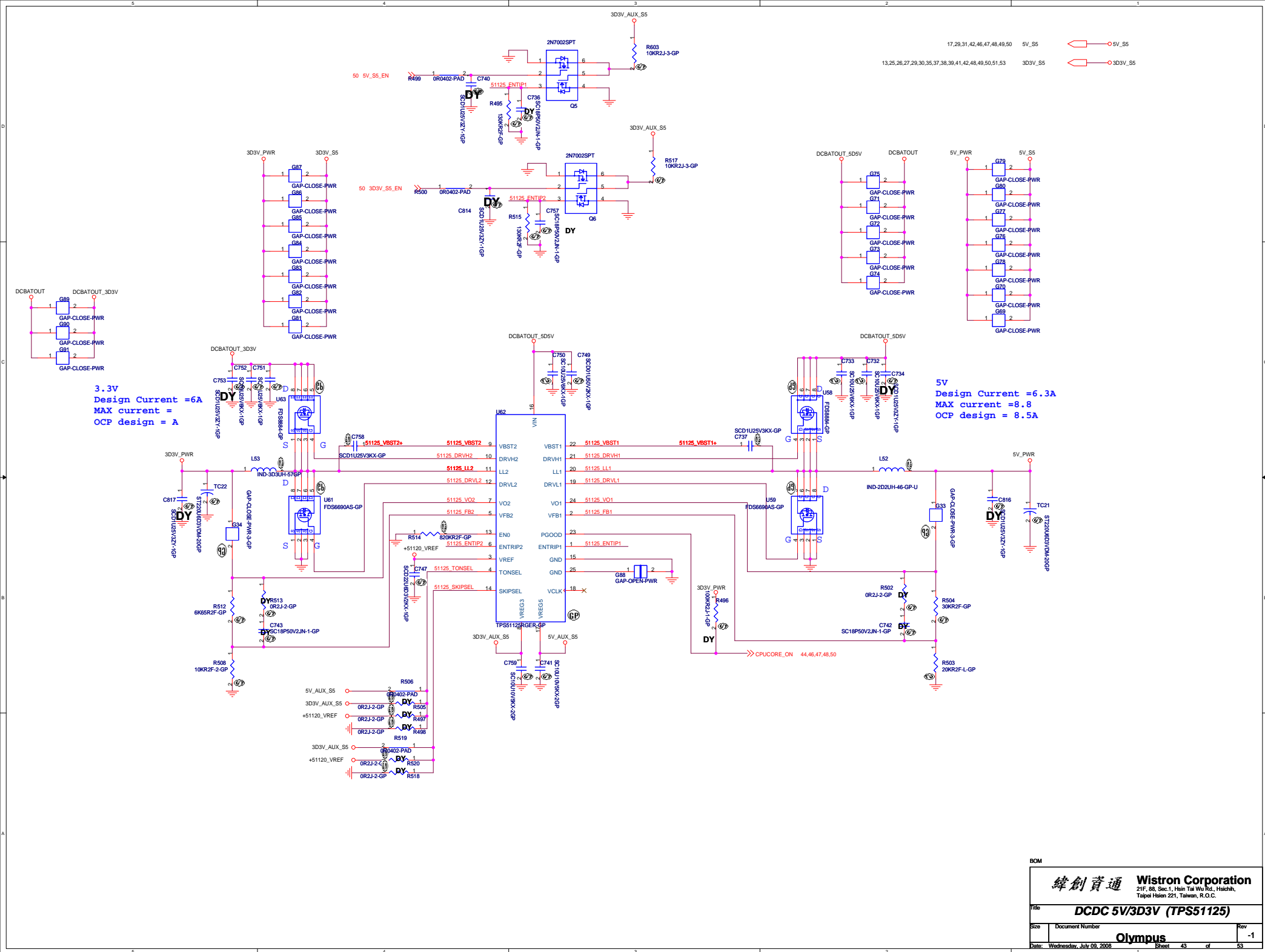


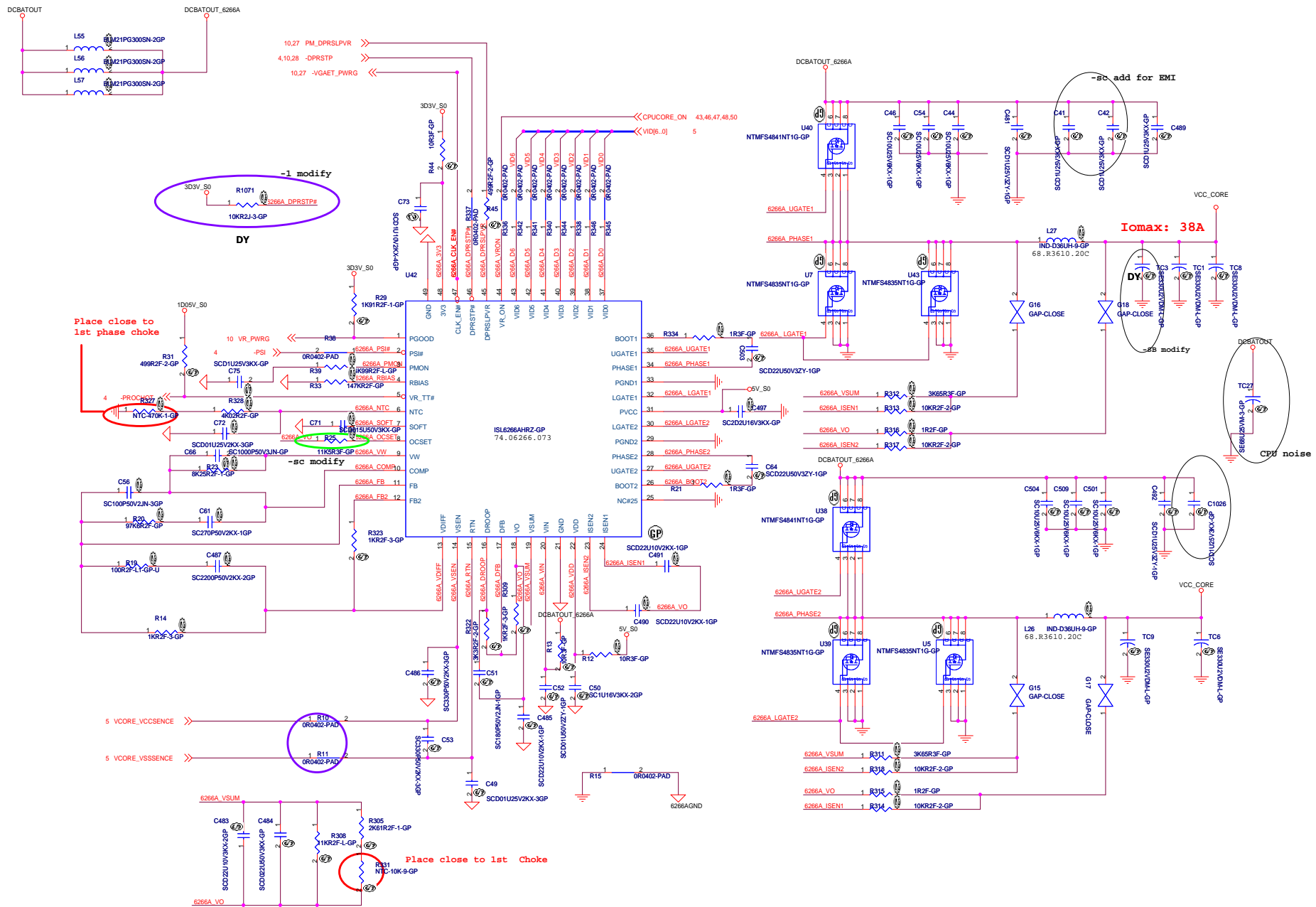
USB*2 + 1394

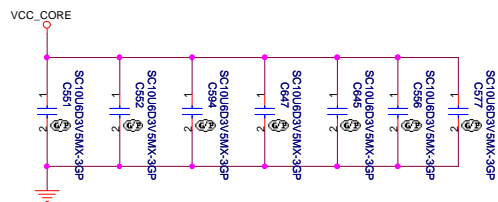


BOM

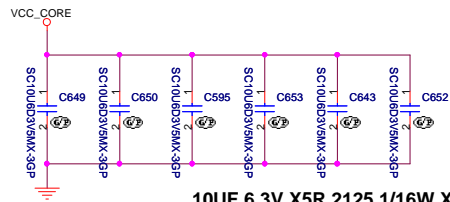
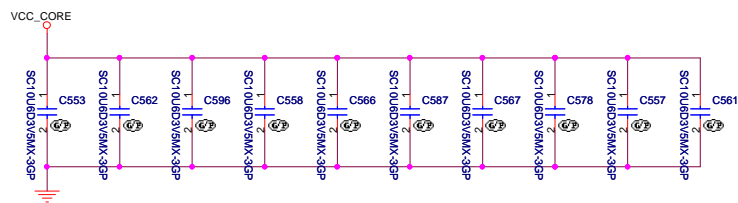
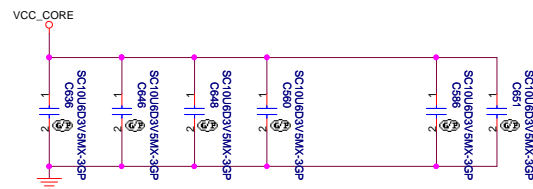
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size		Document Number	
Date: Wednesday, July 09, 2008		Sheet 42 of 53	
USB I/O & 1394 CNN		Rev -1	
Olympus		1	







10UF 6.3V X5R 2125 1/16W X16 PCS



10UF 6.3V X5R 2125 1/16W X16 PCS

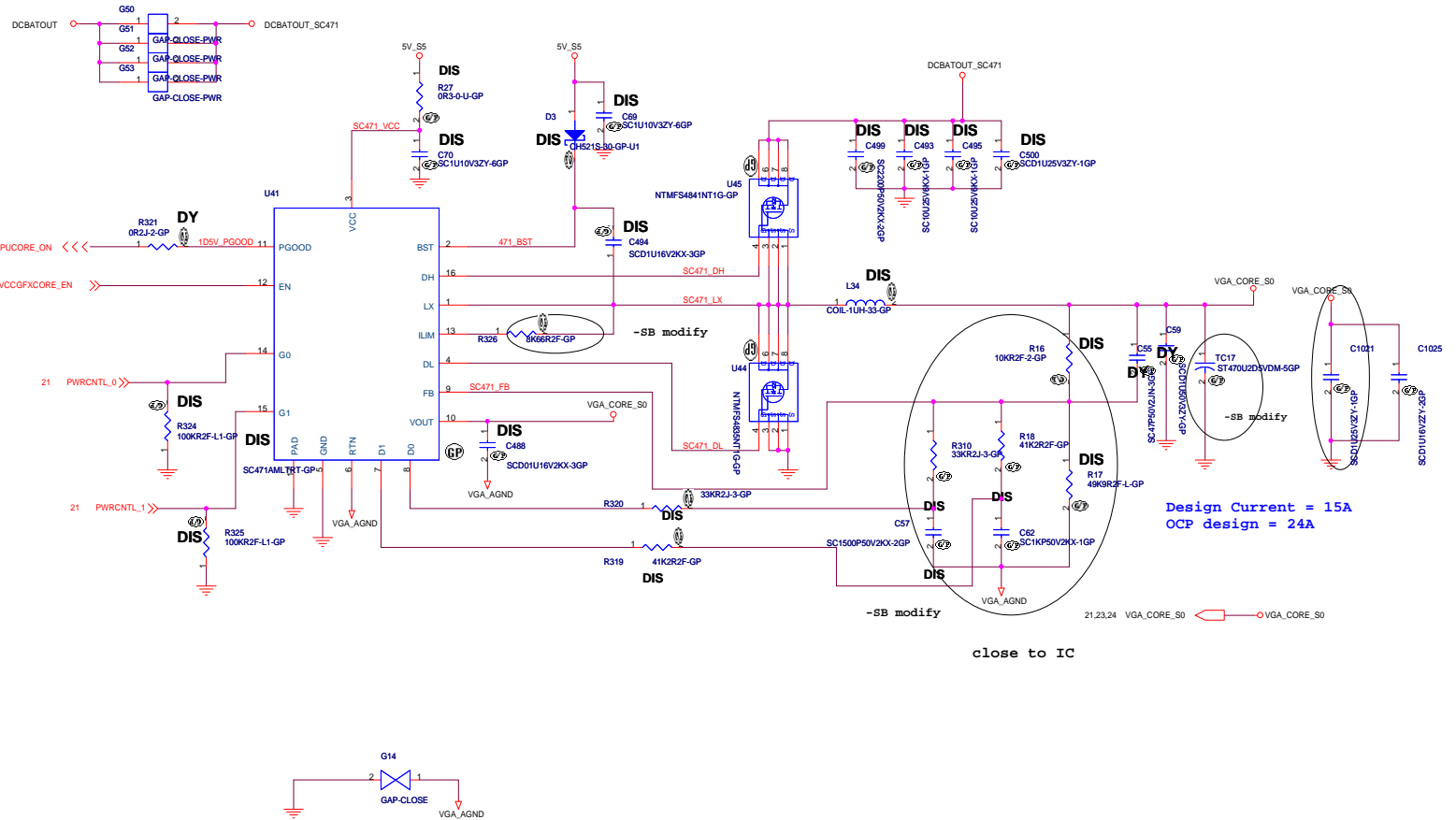
BOM

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		VCCCPUCORE DECOUPLING	
Size Custom	Document Number LT32M	Rev -1	
Date: Wednesday, June 18, 2008		Sheet 45	of 53



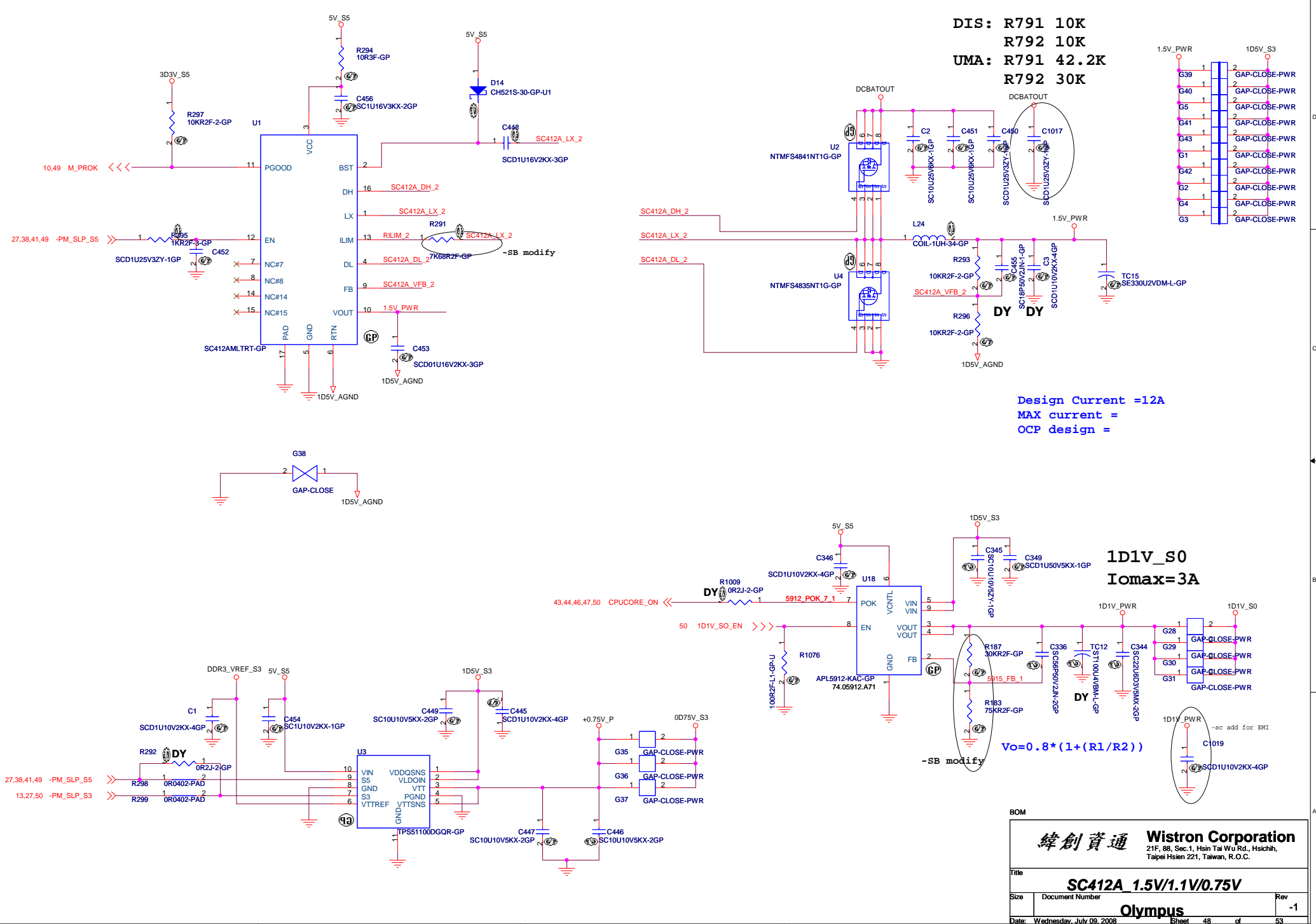
-SB modify

Vout	G1	G0
0.9	1	1
1.0	1	0
0.9	0	1
1.1	0	0



BOM

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
File	
SC471A VGA CORE	
Size	Document Number
C	LT32M
Date: Wednesday, July 09, 2008	Sheet 47 of 53



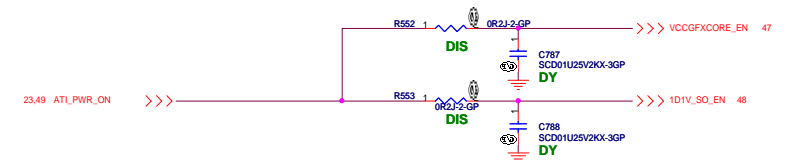
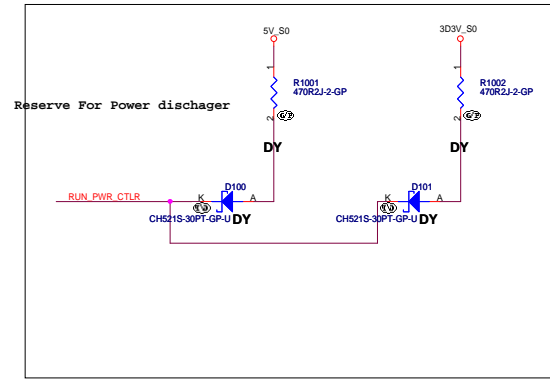
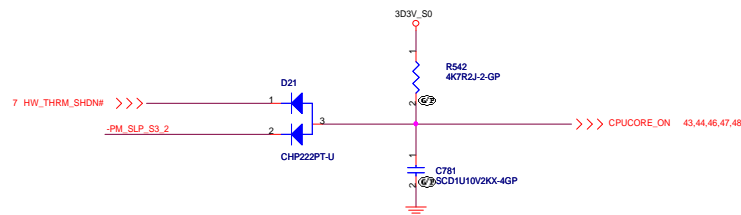
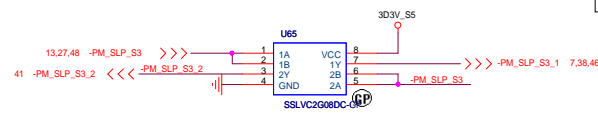
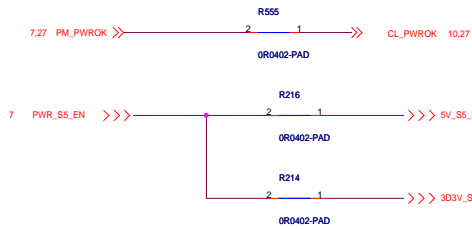
DIS: R791 10K
R792 10K
UMA: R791 42.2K
R792 30K

Design Current =12A
MAX current =
OCP design =

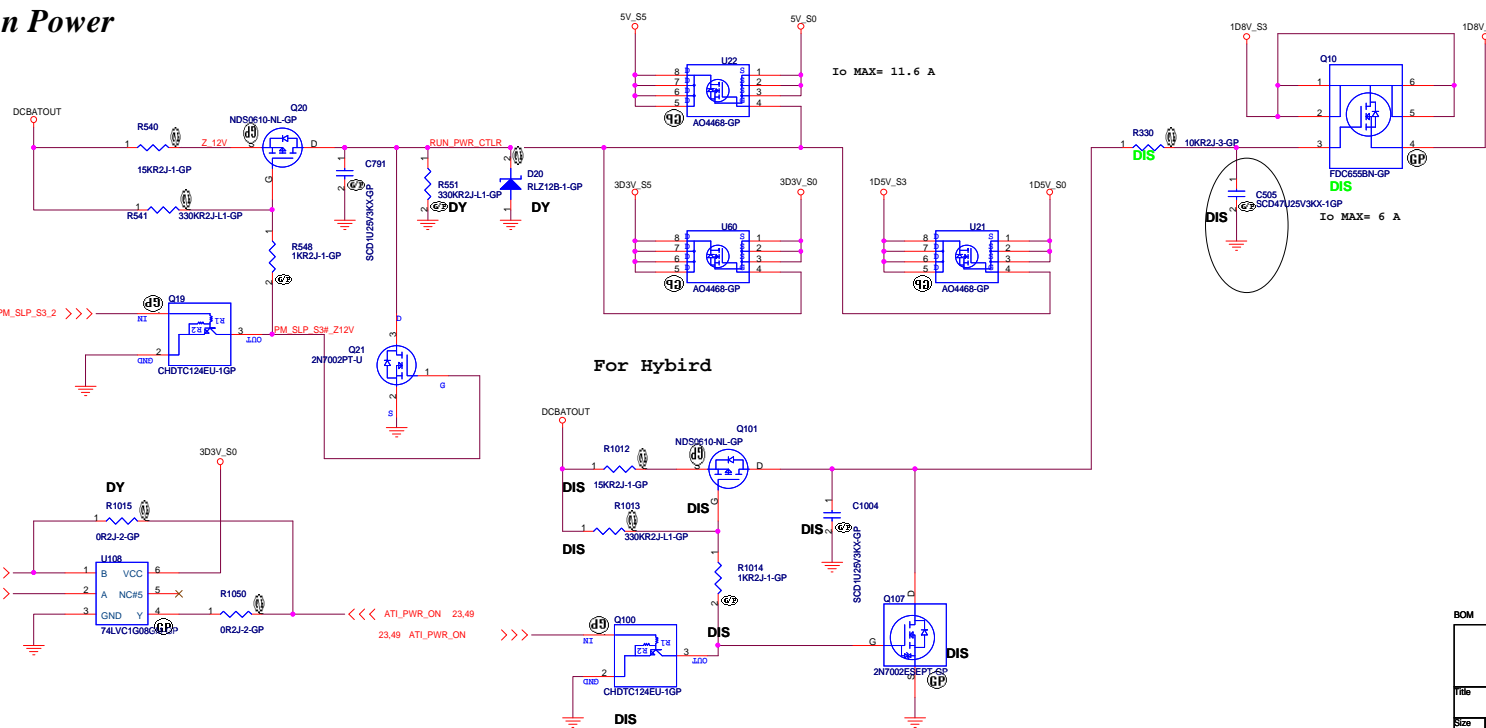
1D1V_S0
Iomax=3A

$$Vo = 0.8 * (1 + (R1/R2))$$

BOM	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
SC412A 1.5V/1.1V/0.75V	
Size	Document Number
Olympus	
Date: Wednesday, July 09, 2008	Sheet 48 of 53
Rev -1	

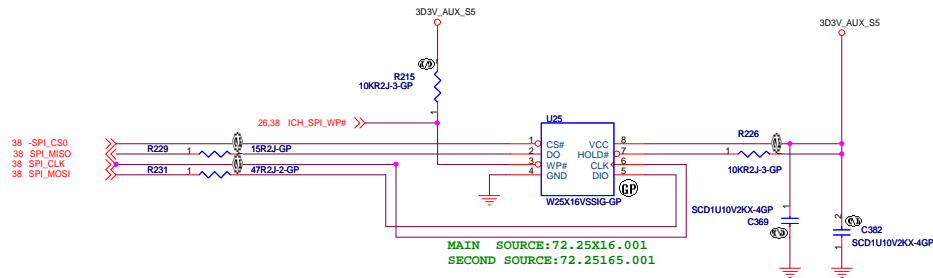


Run Power

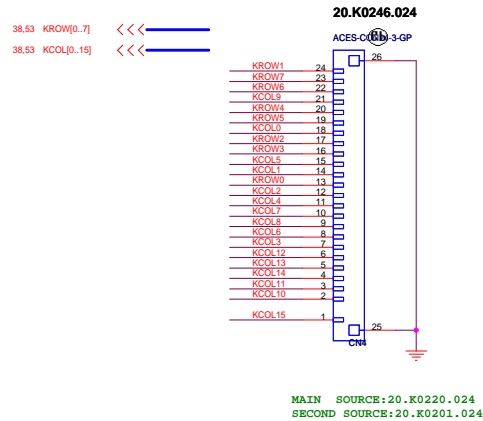


For Hybrid

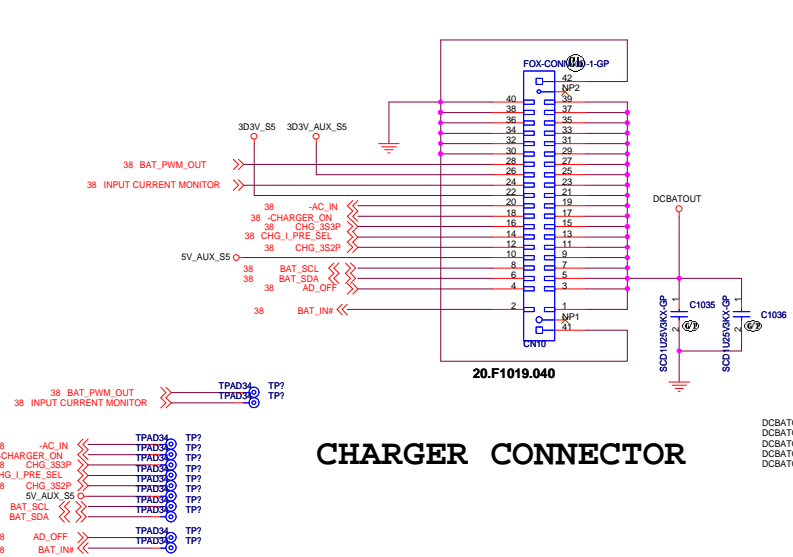
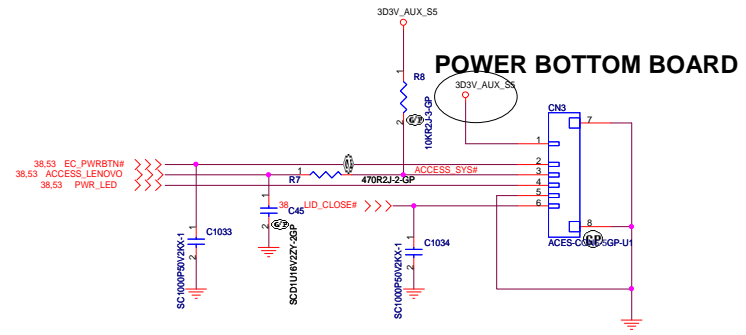
For Hybrid



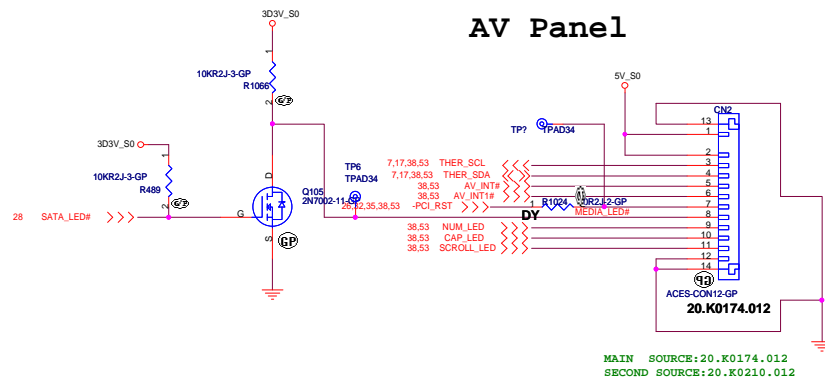
SPI FLASH



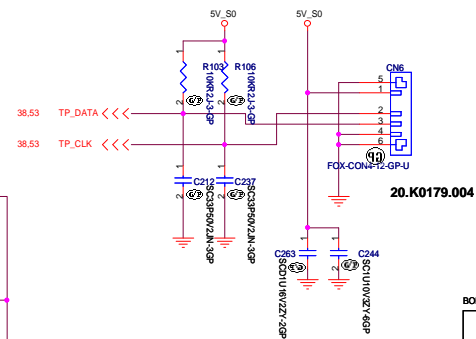
KEYBOARD CONNECTOR

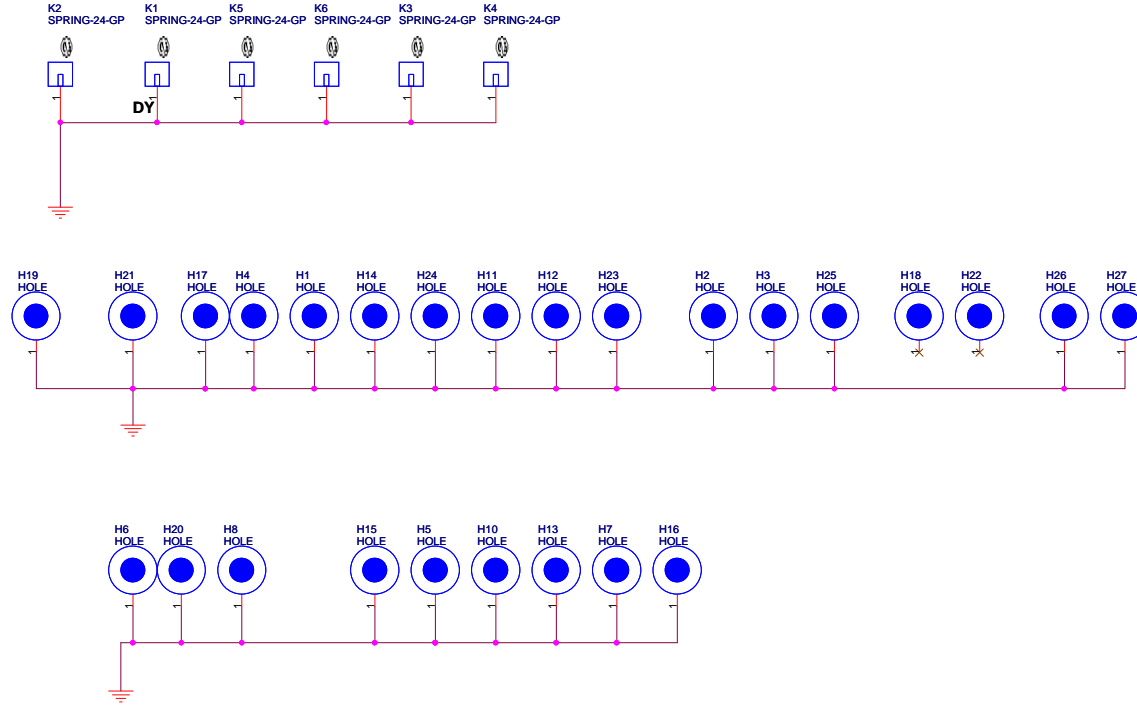


AV Panel



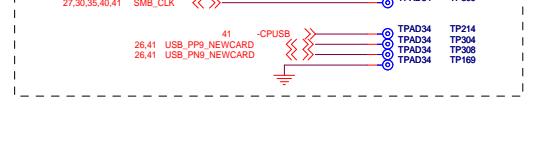
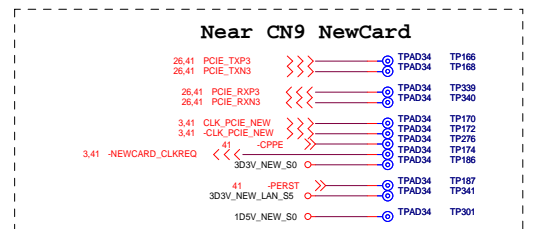
TouchPad Connector





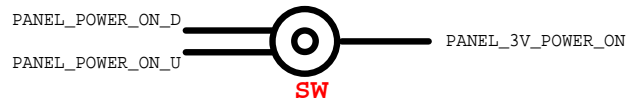
BOM

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		PTH FOR SCREW HOLES	
Size	Document Number	Rev	
Custom		-1	
Date: Wednesday, July 09, 2008		Sheet	52 of 53

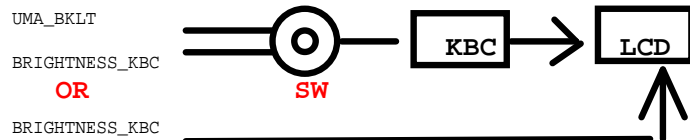


LCD

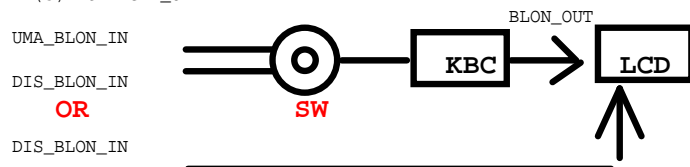
(1) PANEL_3V_ON



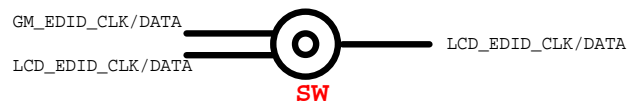
(2) BRIGHTNESS PWM



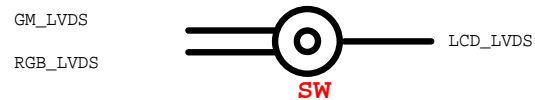
(3) BACKLIGHT_ON



(4) EDID DATA/CLK



(5) LVDS signal



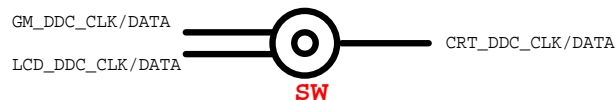
All the switch control by SB_GPIO52
and define

L => -UMA channel

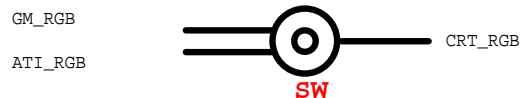
H => -ATI channel

CRT

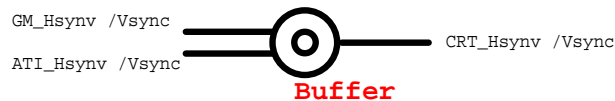
(1) DDC DATA/CLK



(2) RGB signal



(2) Hsync & Vsync



BOM

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>TTEST_PAD</div>			
Size A	Document Number <div>Olympus</div>		Rev -1
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